Innovative dual-side cooled 5x6 PQFN package

Application considerations for best usage

About this document

Scope and purpose

This application note introduces the **SuperSO8** dual-side cooled packaging solution for **OptiMOS™ technology MOSFETs**.

It provides basic information on the differences between dual-side cooled, bottom-side cooled and top-side cooled packages for medium-voltage applications; referring in particular to the 5x6 PQFN package. In addition, it offers some use-case studies to show the benefits of dual-side cooled compared to bottom-side cooled on the system level based on thermal simulations and measurements.

Intended audience

Junior system and hardware engineers and designers of DC-DC converters, switched mode power supplies (SMPS) and driver applications for power tools, who are familiar with the concept of thermal resistance but want to have a slightly deeper understanding.

Senior system and hardware engineers and designers of DC-DC converters, SMPS and driver applications for power tools, who want to understand the benefits and use cases of dual side cooled MOSFETs in more detail.

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1 Introduction

With the increase in power density requirements in AC-DC and DC-DC converters, the role of packaging is changing from the passive pure silicon die envelope used mainly for protection of the silicon die, to a more active role offering actual benefits for new products. In fact, power density can be increased in two ways: the first option is using new silicon technology, which allows a lower $R_{DS(on)}$ per area and better figures of merit (FOMs), decreasing power losses. The second option is to improve the potential for extracting the heat generated by the losses from the device itself. In this case, the packaging technology plays a crucial role.

Recently, more MOSFET manufacturers have been providing options to extract heat from the silicon die more efficiently. When it comes to medium-voltage MOSFET applications, one of the most common packages used is the so-called 5x6 PQFN (SuperSO8). The widespread use of this packaging solution is related to the fact that it has a fairly simple construction and is quite effective in terms of both thermal and electrical performance (such as low electrical parasitic and thermal properties) and provides good reliability (it is mechanically stable, offering good protection for the die).

Figure 1 5x6 PQFN package evolution

Figure 1 shows the evolution of the packaging technology for a 5x6 package commonly used in medium-voltage applications, from the initial SO8 without exposed pad to the SuperSO8 dual-side cooling.

An important parameter by which to assess the efficiency of power extraction from the die is the thermal resistance R_{th}; the lower this number is, the better the capability to remove the heat generated in the device by the losses and therefore, this is the parameter that shows how good the package is in helping the device to work at a lower temperature. In the case of the 5x6 PQFN there are two possible paths for the heat from the junction, where the power dissipation is located, to the ambient: toward the bottom and toward the top. In the first approximation, the lateral contribution, due to the small areas, can be ignored. Consequently, two numbers are relevant when judging the packaging technology from thermal resistance point of view:

a) $R_{thJC(top)}$: Thermal resistance from the junction to the top of the package
b) $R_{thJC(bot)}$: Thermal resistance from the junction to the bottom of the package

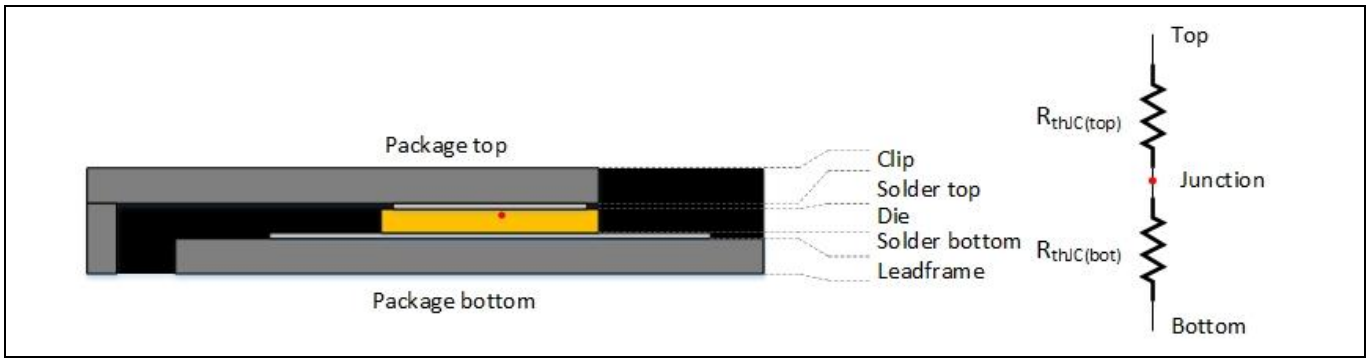


Figure 2 Thermal resistances location

Introduction

Figure 2 shows a simplified electrical-equivalent thermal network for a modern PQFN package employing a copper clip, where the thermal resistances listed above represent the main paths for the heat (picture not to scale). The $R_{thJC(top)}$ is formed by the silicon die, the top layer of solder and the clip; the $R_{thJC(bot)}$ is formed by the silicon die, the bottom layer of solder and the leadframe.

Table 1 Comparison of thermal resistances for different packaging technologies

Package	$R_{thJC(top)}$ [K/W]	$R_{thJC(bot)}$ [K/W]	Definition
SO8	10 to 20	10 to 20	
SuperSO8	10 to 20	0.5 to 5	bottom-side cooled
SuperSO8 dual-side cooled	0.7 to 5	0.5 to 5	dual-side cooled

Table 1 shows the typical values reported in the datasheets of the three different packaging technologies. Those numbers might differ from manufacturer to manufacturer due to the definition of thermal resistance, the measurement method for the thermal resistance, and device characteristics. What is relevant is the order of magnitude of the thermal resistance itself. These numbers help us to categorize the different types of cooling method; at the time of writing, typical values for good thermal resistance in the 5x6 package are in the range of 0.5 to 5 K/W.

A low thermal resistance from junction to top and from junction to bottom qualify a package as dual-side cooled. Here, “low” is arbitrarily considered a value lower than 5 K/W.

In case a package has one of the two paths with a much lower thermal resistance compared to the other (here, 1/10 is considered “lower”), it will be described as either top-side cooled or bottom-side cooled.

From the above numbers it seems clear that a designer who wants to increase the power density should use a Dual Side Cooled device, since the advantage of the thermal resistance from junction to top compared to the SuperSO8 is quite significant, at roughly five times lower.

This application note will show that such a large difference is not always reflected in an equally as large improvement in application. Furthermore, in some cases the improvements are not related to the thermal resistance but rather to the thermal dynamic behavior. In other words, the two solutions – SuperSO8 bottom-side cooled and SuperSO8 dual-side cooled– provide similar thermal resistance in application, though they show very different behavior in terms of thermal capacitance.

2 Product description

Infineon Technologies offers many different options for cooling MOSFETs. **Figure 3** shows the broad portfolio of SMD packaging technologies designed for 5x6 packages and other sizes. This wide range enables customers to design converters with the most suitable packaging solution according to their needs.

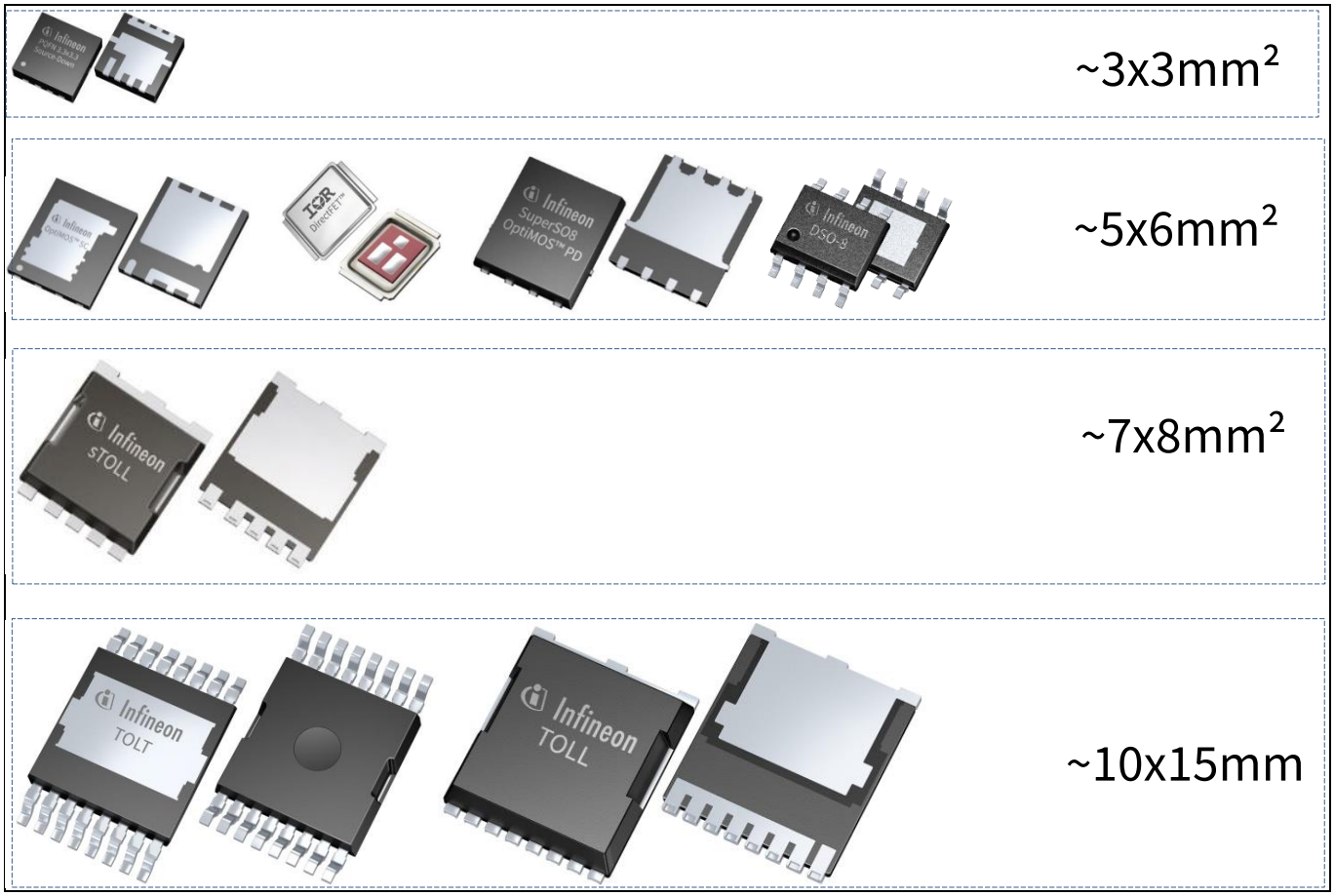


Figure 3 Different SMD cooling package options

One of the many options is to use the 5x6 PQFN dual-side cooled as a power density booster for the 5x6 PQFN bottom-side cooled (standard SuperSO8). **Figure 4** shows how it is possible to unify the landing pattern of the bottom-side cooled and the dual-side cooled in such a way that it can host both packages. This feature allows customers to switch from one package technology to the other, seamlessly. This can be useful where customers would like to increase the power density of a power supply or converter with little effort, simply by replacing the bottom-side cooled with the dual-side cooled counterpart and adding a heatsink.

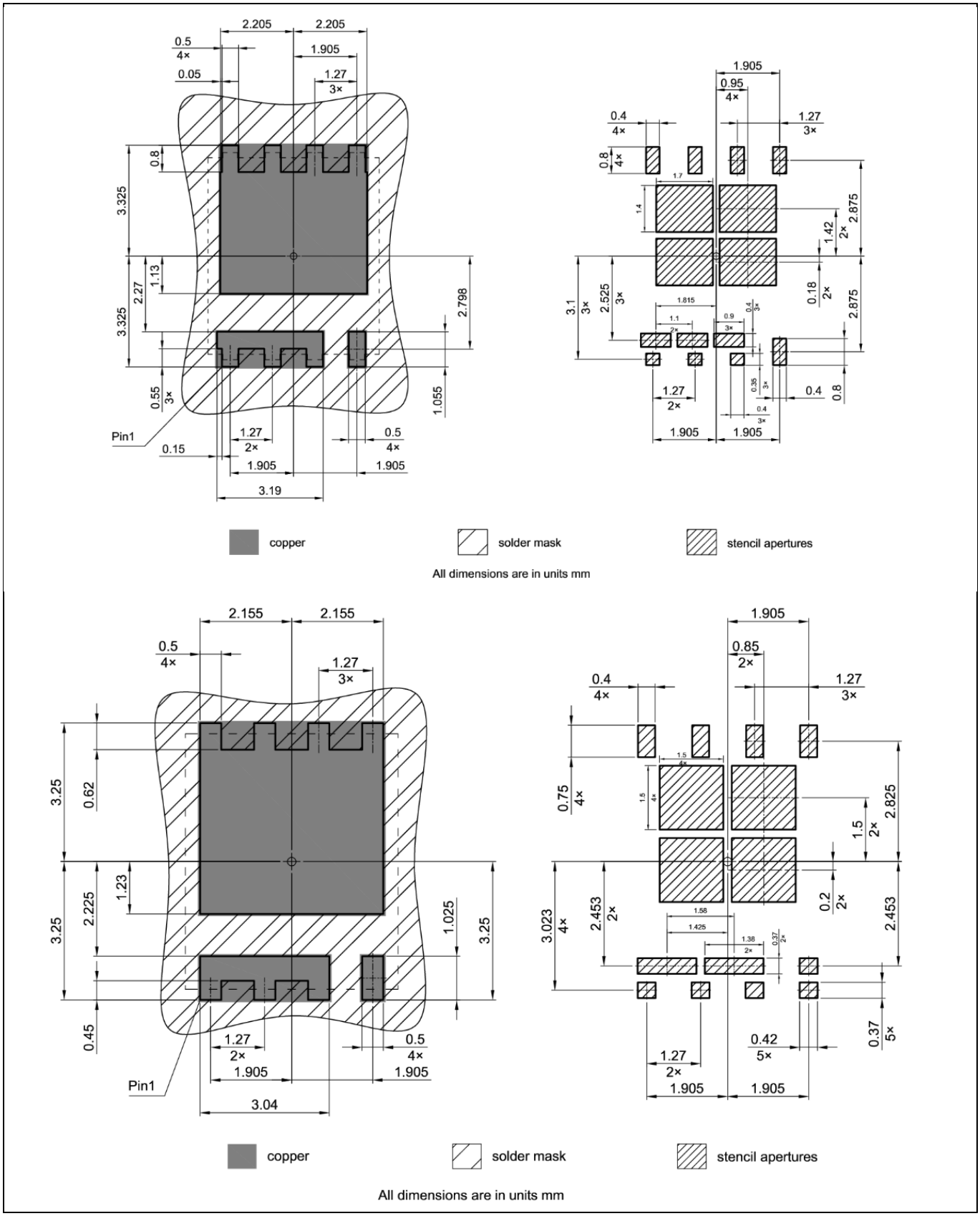


Figure 4 **Footprint dimensions, board pads and stencil apertures (top: bottom-side cooled, bottom: dual-side cooled)**

Table 2 Product portfolio

$R_{DS(on)}$ [mΩ] (max.)	V_{DS} [V]	5x6 PQFN bottom-side cooled	5x6 PQFN dual-side cooled
0.7	40	BSC007N04LS6	BSC007N04LS6SC
0.9	40	X	BSC009N04LSSC
1.4	60	BSC014N06NST	BSC014N06NSSC
1.6	60	BSC016N06NST	BSC016N06NSSC
2.8	60	BSC028N06NST	BSC028N06NSSC
2.3	80	X	BSC023N08NS5SC
3.3	80	X	BSC033N08NS5SC
3	100	X	BSC030N10NS5SC
4	100	BSC040N10NS5	BSC040N10NS5SC
7	100	BSC070N10NS5	BSC070N10NS5SC
9.3	150	BSC093N15NS5	BSC093N15NS5SC
11	150	BSC110N15NS5	BSC110N15NS5SC
16	150	BSC160N15NS5	BSC160N15NS5SC

The potential for swapping the device easily from bottom-side cooled to dual-side cooled is not only related to the fact that they share the same footprint, but also, as **Table 2** shows, to the compatibility of the product portfolio. In fact, for every bottom-side cooled device there is a counterpart in the dual-side cooled devices with exactly the same electrical characteristics. This is a great advantage for customers who need to qualify a product during the new design evaluation and verification process. With a one-to-one replacement there will only be the need for thermal verification of the new solution based on the dual-side cooled, since the evaluation of the electrical product performance has already been conducted during the qualification process of the bottom-side cooled.

The only relevant difference between the dual-side cooled product and the bottom-side cooled product that should be considered during the PCB layout phase is related to the height. In fact, the dual-side cooled has a typical height in the range of 0.5 mm, while the bottom-side cooled is more in the range of 1 mm; the package fabrication process is partially responsible for this lower height, and the next paragraph briefly describes that process. However, the fabrication process is not the only factor. In fact, a slightly different approach could have been used: for instance, a different clip thickness or a compensating metal layer could have been inserted to reach the final height of 1 mm.

This kind of solution has been purposely avoided for several reasons. First, the height compatibility between bottom-side cooled and dual-side cooled is not a specific requirement. For instance, it is counterintuitive in a SMPS to exchange only some of the synchronous rectifiers from bottom-side cooled to dual-side cooled, and to add the heatsink without also exchanging other parts, which might limit the height of the heatsink. More generally, MOSFETs operating in the same function will have the same requirements; therefore, it is quite unlikely that there will be a mixture of dual-side cooled and bottom-side cooled devices and consequently a mixture of different heights.

Furthermore, the insertion of a metal layer between the clip and the top of the package, again to accommodate the 1 mm thickness, decreases the device performance in terms of thermal resistance. Looking again at **Figure 2**, the reason for that becomes clear. The thermal resistance from junction to top is a function of different geometrical characteristics of the clip. The most relevant is the distance between the die and the top of the package. The greater the distance, the higher the thermal resistance between the junction and the top of

the component. Therefore, the insertion of a middle layer between the clip and the top of the package to compensate for the height difference would degrade a key parameter of the new packaging technology.

Finally, Infineon Technologies has decided to use the suffix “SC” to identify dual side cooled products as distinct from die technology and package type.

2.1 Product construction

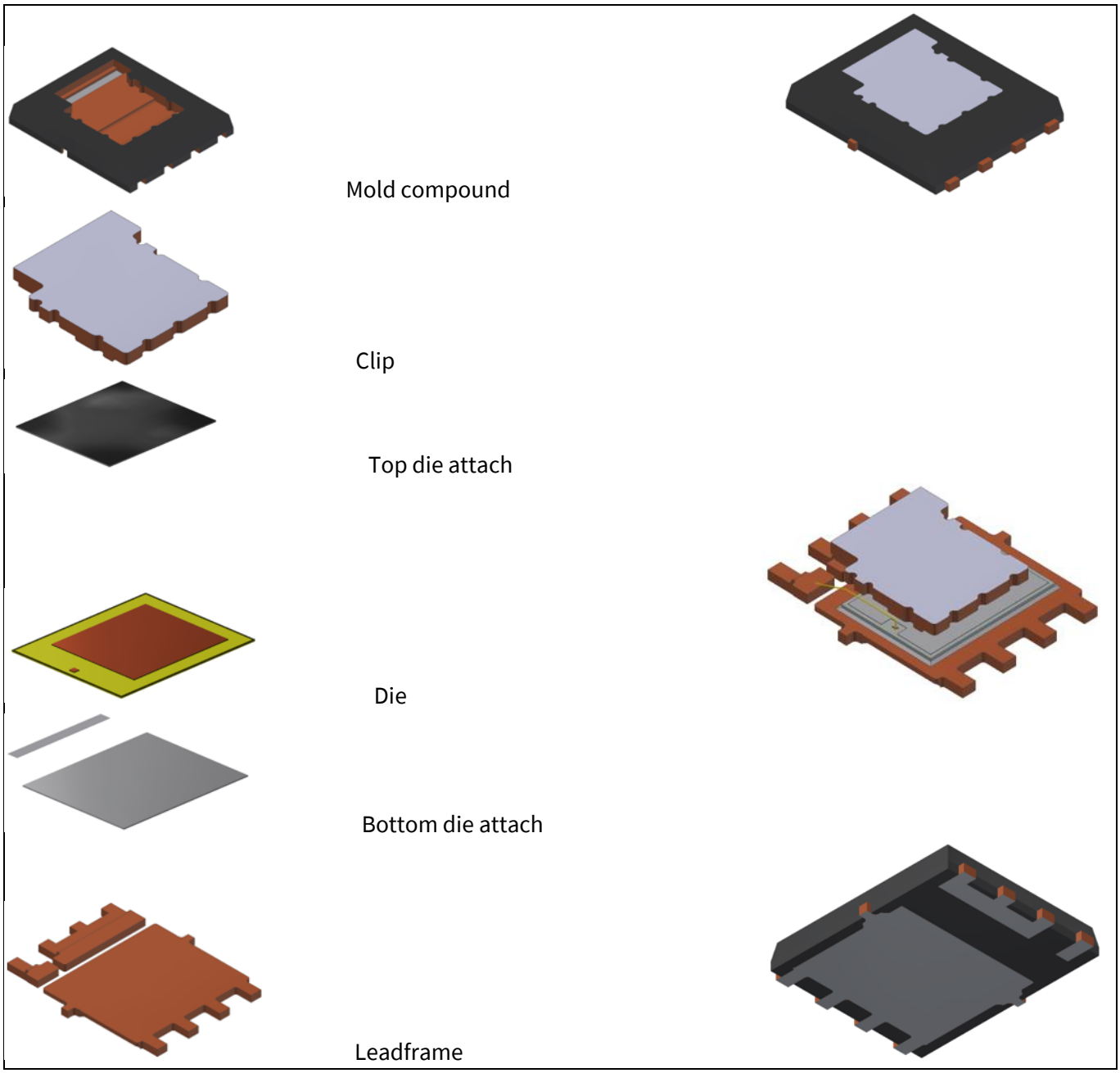


Figure 5 Dual-side cooled product construction – composition (left) and final result (right)

Figure 5 shows the product construction. The basic technology is the same as the bottom-side cooled and it includes the following components: lead frame supporting the die, die attach, die passivation and opening, clip attach and mold compound.

If the construction is very similar, the process to produce the component is more complicated for several reasons. The first relates to the fact that the exposure of the clip to the top of the package is not as simple as it might seem at first glance. It is very important that the clip stands out from the mold compound, otherwise the attachment of the heatsink might not reach the clip itself. The second reason is the fact that in a bottom-side cooled the main purpose of the clip is to provide the source connection of the device, bringing the current from the top of the device to the bottom. In the dual-side cooled solution, the clip not only has the function of realizing a low-ohmic connection between the silicon die source and package pin source, but also the goal of creating a good thermal path for the heat. Although normally current conduction and heat conduction lead to solutions that are optimal for both, in some cases different optimization priorities lead to different solutions, for example for easier production flow. In the case of the dual-side cooled, the opening in the passivation layer to connect the clip is maximized, so that the heat conduction to the top of the device is optimal; this requires different production steps compared to the bottom-side cooled, which make the production process more complicated.

2.2 Relevant product parameters

Since the electrical properties are the same as the bottom-side cooled counterpart, the most important parameters of the dual-side cooled are the thermal resistances. Infineon Technologies has paid careful attention to designing the top-side cooling path in order to minimize the $R_{thJC(top)}$.

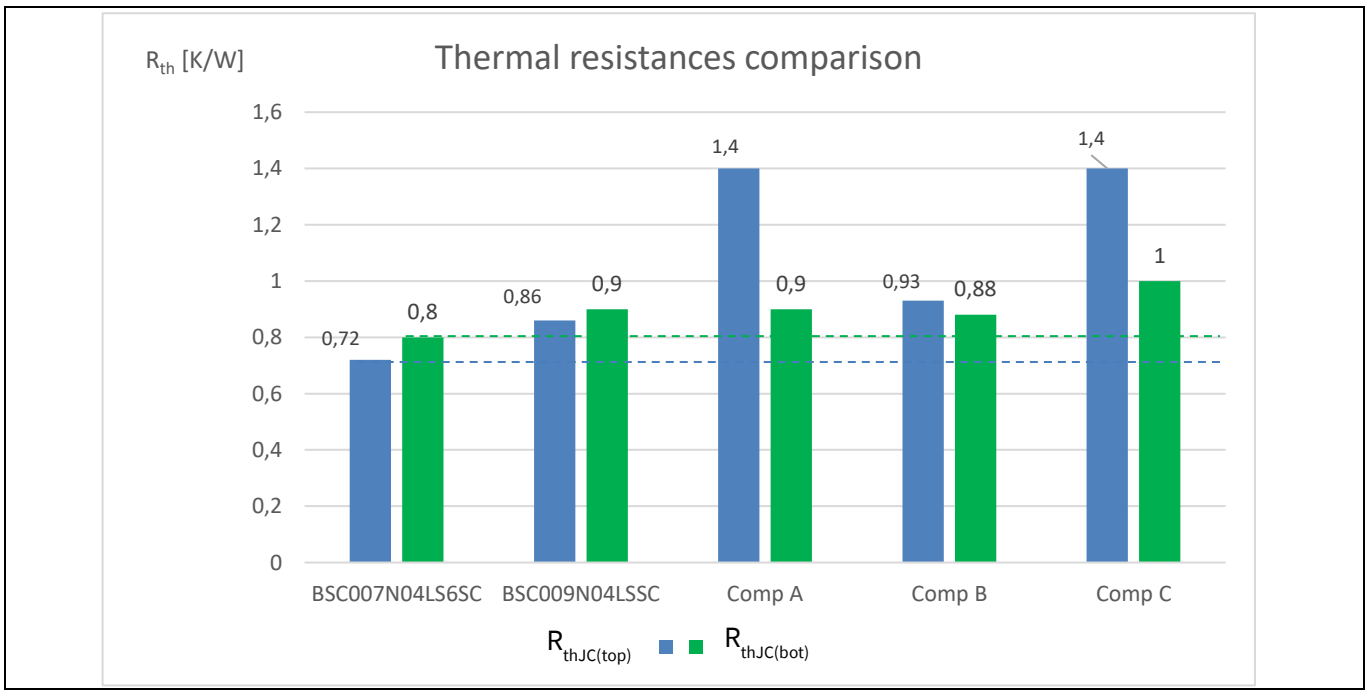


Figure 6 Thermal resistance comparison between dual-side cooled 5x6 packages

A direct comparison with competitors' devices is not possible because of slightly different $R_{DS(on)}$ values, but **Figure 6** shows a comparison based on datasheet values between low-$R_{DS(on)}$ devices for the 40 V V_{DS}.

Infineon Technologies offers the lowest thermal resistances; roughly 30 percent lower compared to the nearest competitor for $R_{thJC(top)}$. Due to careful optimization Infineon can even thermally outperform some competitors' best-in-class devices with devices that are not considered best-in-class.

3 Product performance

3.1 Thermal performance

3.1.1 Standalone thermal performance

In many cases, measurements or simulations are the best way to show improvements related to the dual-side cooled adoption. Since this is a product comparison, the conditions for the simulations and for the measurements are normally product related. **Figure 7** helps to explain the concept.

The overall thermal resistance is given by:

$$Rth_{JA} = \frac{(Rth_{TA} + Rth_{TIM} + Rth_{JC(top)}) * (Rth_{JC(bot)} + Rth_{BA})}{(Rth_{TA} + Rth_{TIM} + Rth_{JC(top)} + Rth_{JC(bot)} + Rth_{BA})}$$

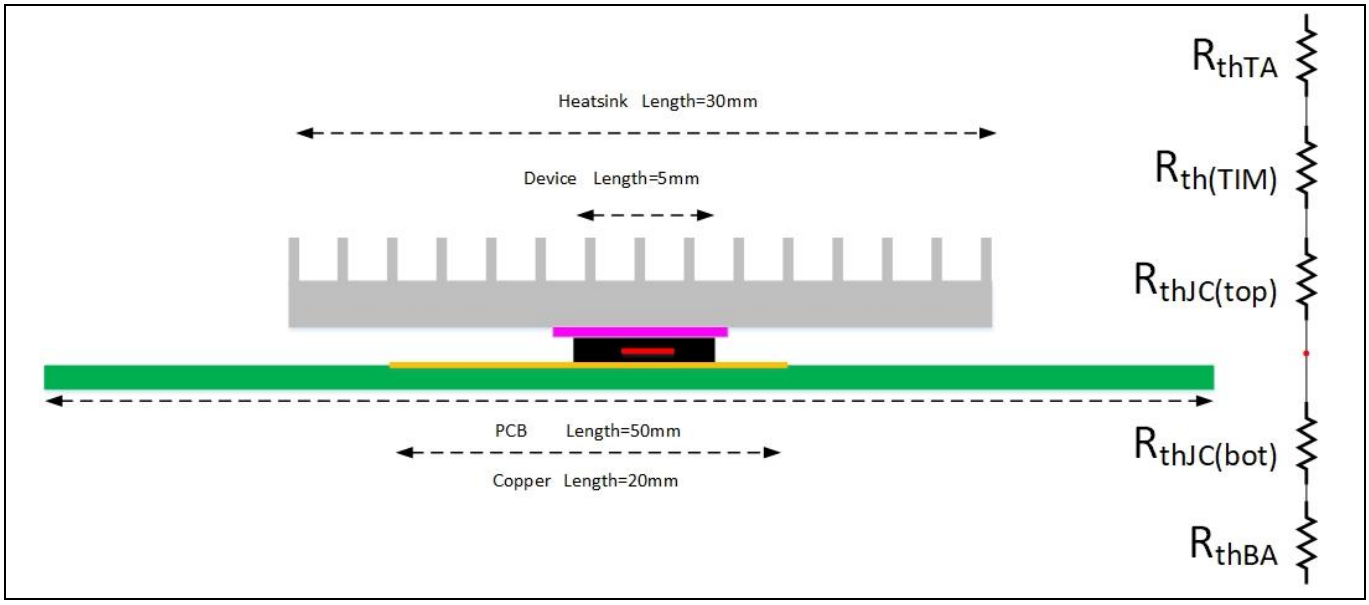


Figure 7 Proportions between the different lengths

As pointed out in references [1], [2] and [3] as well in **Figure 7** (scaled only in the horizontal direction), the board and the heatsink used to make either the simulations or the measurements are quite large, compared to the single device. This setup influences the thermal resistances of the system (formed by the thermal resistance from junction to ambient top and the thermal resistance from junction to ambient bottom) and therefore the improvements in the exchange from bottom-side cool to dual-side cool. This is related to the fact that thermal resistance at the system level (device, PCB and heatsink) is different from the thermal resistance of the device alone. Analyzing this in more detail, as in the three references, it can be seen that:

- In [1] there is no immediate information on the size of the PCB and the size of the heatsink. There is instead interesting information about the thermal resistances of different packaging technologies and, as pointed out in the previous paragraph, the gap between a bottom-side cooled and a dual-side cooled package in terms of $R_{thJC(top)}$ is in the range of 10 times smaller values for the dual-side cooled (~1 K/W vs. 10 K/W). Despite the huge difference in terms of thermal resistance from junction to top at the device level, the gain in terms of temperature and current decrease is in the range from 20 to 30 percent. As just stated, this is because the thermal resistance of the heatsink and/or PCB is much higher than the thermal resistance of the device itself.

- [2] provides a lot more information on the sizes of the PCB and heatsink. The PCB is roughly 2500 mm² (the copper area is not clear, but possibly around 300 mm²) and the heatsink is roughly 900 mm². Considering that the product itself is 30 mm², this is clearly a big difference. In this case, the gain in terms of temperature reduction is more noticeable, roughly 50 percent. In this case the gain in terms of temperature is greater, since the thermal resistance of the system is in the same range as the device thermal resistance.
- [3] makes more information available on the size of the PCB, amount of copper and size of the heatsink. In this case, different heatsinks are also used. In the end, one of the heatsinks was roughly 1800 mm² and the other was 625 mm². In this case, the maximum gain in power dissipation is also in the range of 60 percent (60 percent more power for the dual-side cooled in comparison with either the SO8 or bottom-side cooled). Again, the thermal resistance of the added parts (heatsink and PCB) is in the same range as the device thermal resistance.

In addition, Infineon Technologies has done simulations at the product level to prove the benefits of dual-side cooled. In this case, the heatsinks used are smaller, compared to the previous articles.

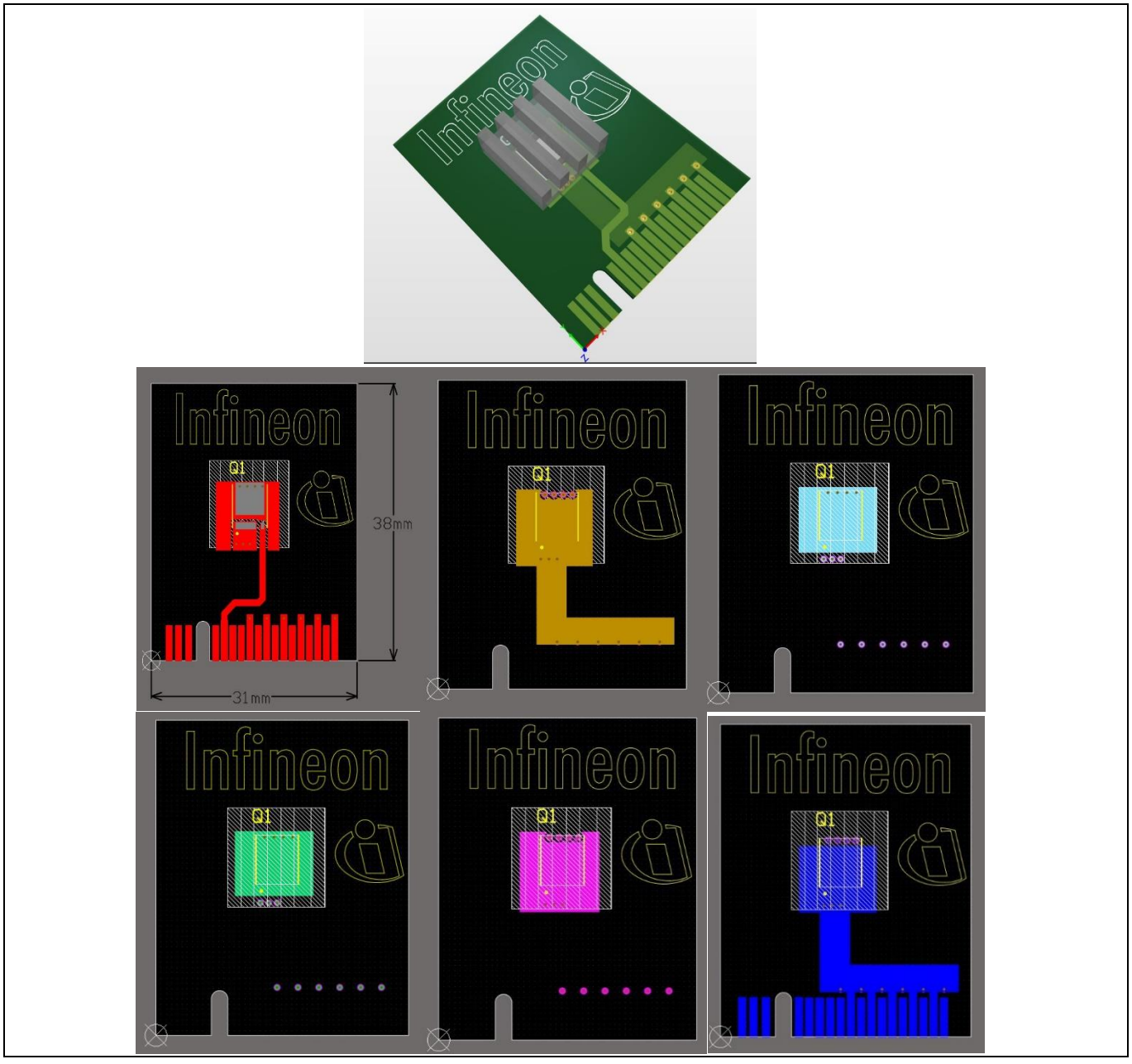
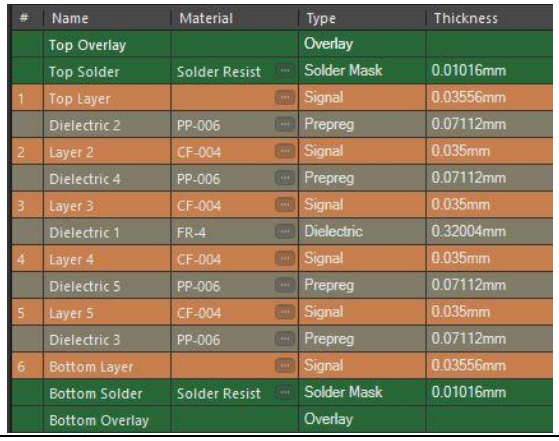


Figure 8 Board and layer designs used for thermal simulation on the product level

Figure 8 shows an isometric view of the PCB and the different layers of the layout. From top left clockwise: top layer, layer 2, layer 3, layer 4, layer 5 and bottom layer. For clarity the dual-side cooled package is shown.



#	Name	Material	Type	Thickness
	Top Overlay		Overlay	
	Top Solder	Solder Resist	Solder Mask	0.01016mm
1	Top Layer		Signal	0.03556mm
	Dielectric 2	PP-006	Prepreg	0.07112mm
2	Layer 2	CF-004	Signal	0.035mm
	Dielectric 4	PP-006	Prepreg	0.07112mm
3	Layer 3	CF-004	Signal	0.035mm
	Dielectric 1	FR-4	Dielectric	0.32004mm
4	Layer 4	CF-004	Signal	0.035mm
	Dielectric 5	PP-006	Prepreg	0.07112mm
5	Layer 5	CF-004	Signal	0.035mm
	Dielectric 3	PP-006	Prepreg	0.07112mm
6	Bottom Layer		Signal	0.03556mm
	Bottom Solder	Solder Resist	Solder Mask	0.01016mm
	Bottom Overlay		Overlay	

Figure 9 PCB layer thicknesses and materials

Figure 9 shows the properties of the PCB in terms of number of layers (six), copper thickness of the layers (35 µm), dielectric thickness (70 µm) and core thickness (320 µm).

The vias used in the board have the following characteristics:

- Hole size: 0.4 mm
- Pad diameter: 0.7 mm
- Wall thickness: 23 µm

Table 3 Heatsink characteristics (height includes the base)

	HS1	**HS2**
Dimensions [mm^3]	8x8x6	11.8x8x8
Base thickness [mm]	2	2.5
Number of fins	5	4
Fin pitch [mm]	0.9	1.7
Fin width [mm]	0.9	1.7

Table 3 shows the heatsink characteristics; **Figure 8** uses the HS2.

Table 4 Thermal resistance – junction ambient

Airflow [m/s]	**bottom-side cooled**			**dual-side cooled**		
	W/O HS	HS1	HS2	W/O HS	HS1	HS2
	R_{thJA} [K/W]			R_{thJA} [K/W]		
0	71	60	54	71	59	52
1	50	38	31	49	37	30
2	42	31	25	42	30	24
3	37	28	**23**	37	27	**20**

In this case, the improvements between bottom-side cooled and dual-side cooled are even smaller than compared to the previous cases, due to the small dimensions of the heatsink used in the experiment, which limits the thermal performance.

All the tests were performed with an ambient temperature of 25°C and with the board placed vertically with natural airflow in the direction of the fins.

Figure 10 Setup used for test results in Table 4 (bottom-side cooled)

This approach – considering an enormous PCB and heatsink – is absolutely acceptable and dictated by a comparison based on the product level, which harmonizes the conditions and simplifies the process of the assessment to quantify the benefits. In fact, there are too many variable conditions for different applications to be covered to prove the improvements of the dual-side cooled. The results of the comparison obtained in this way provide a quantification of the improvements, but this might be too poor (as seen in **Table 4**) or too far away from the real conditions (as seen in [**1**], [**2**] and [**3**]) to be considered realistic. Those considerations lead to the point of evaluating the performance in a more application-relevant environment.

3.1.2 Thermal performance in application – simulation

As seen in the previous paragraph, depending on boundary conditions an improvement in the operating temperature of between 20 and 50 percent can be achieved using top side cooling device. The assumption behind those results is the use of a large PCB and heatsink. This paragraph will consider a more realistic condition, closer to the application condition, for analyzing the improvement of the dual-side cooled compared to the bottom side cooling.

Power tools are a growing market, benefiting from the trend for “electrification”, which has been gaining momentum since the beginning of the millennium.

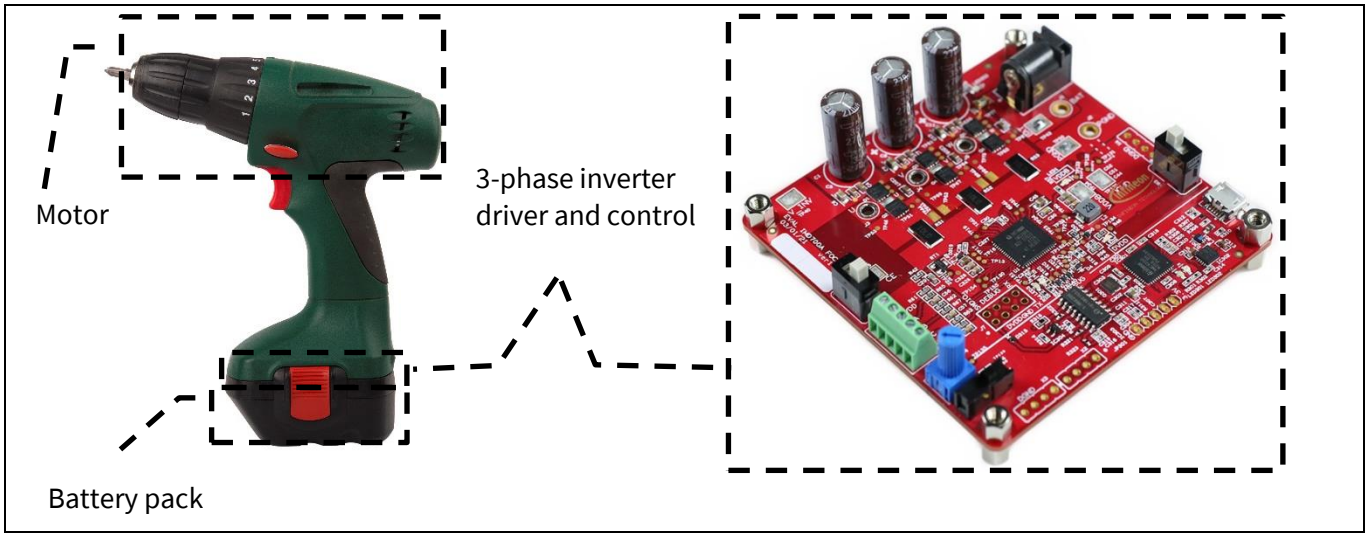


Figure 11 Power tool and Infineon Technologies evaluation kit

Figure 11 shows the application considered together with the essential components: battery, motor and three half-bridges (HBs) to control the motor spinning speed and torque; it also shows the **EVAL_IMD700A_FOC_3SH** [4], Infineon Technologies' evaluation kit. Because the tools need to be portable, not much weight and space can be taken up by the power board. This means that the space reserved for the electronics and for the heatsink is minimal, and much smaller than the equivalent space reserved in the SMPS applications, for instance.

In order to assess the benefits of the dual-side cooled in comparison with the bottom-side cooled simulations considering those boundary conditions have been performed.

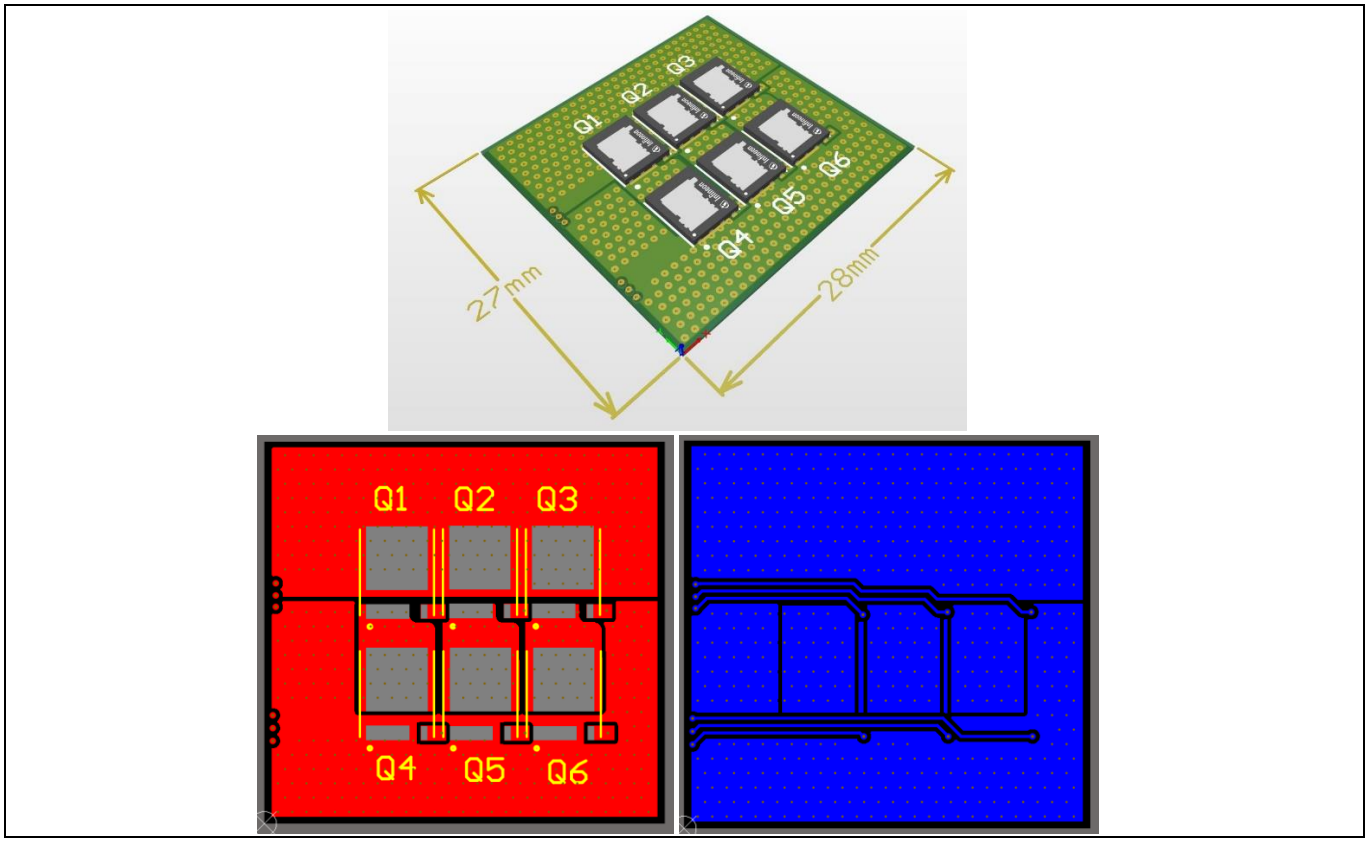


Figure 12 Board setup and layout used for thermal simulations

Figure 12 shows the layout of the three HBs only in relation to the power path, from the battery to the three HBs and to the motor with the three different phases. In order to make the simulation simpler the connectors for the battery and for the three phases to the motor are not considered. Furthermore, the parts dedicated to the control logic and the driving circuitry are not included. The board is equipped with as many vias as possible to make it work reasonably well in terms of heat transfer from top to bottom, but this is not always the case, since vias add cost to the production.

The PCB is essential, as in the real application. As shown, the PCB is slightly larger than the size of the power components, and furthermore the PCB employs only two layers with 35 µm copper. The hole of the via is 0.2 mm and the diameter is 0.4 mm; the pitch is roughly 1 mm. The size of the board is 27 mm x 28 mm. To complete the description of the PCB, the overall thickness is roughly 0. 5 mm, with a core of 0.32 mm.

In power tools there is not much room for a finned heatsink; it is also quite unlikely, depending on the size of the tool and its use, that there will be airflow inside the system. In many cases, the metal case of the tool is used as a heatsink; in other cases, a very simple slab of metal can be used as a heatsink too. For these reasons, the simulation setup considers a metal case slightly larger than the PCB, which will also be used as mechanical support for the PCB. The PCB is surrounded with a plastic container of 1 mm thickness.

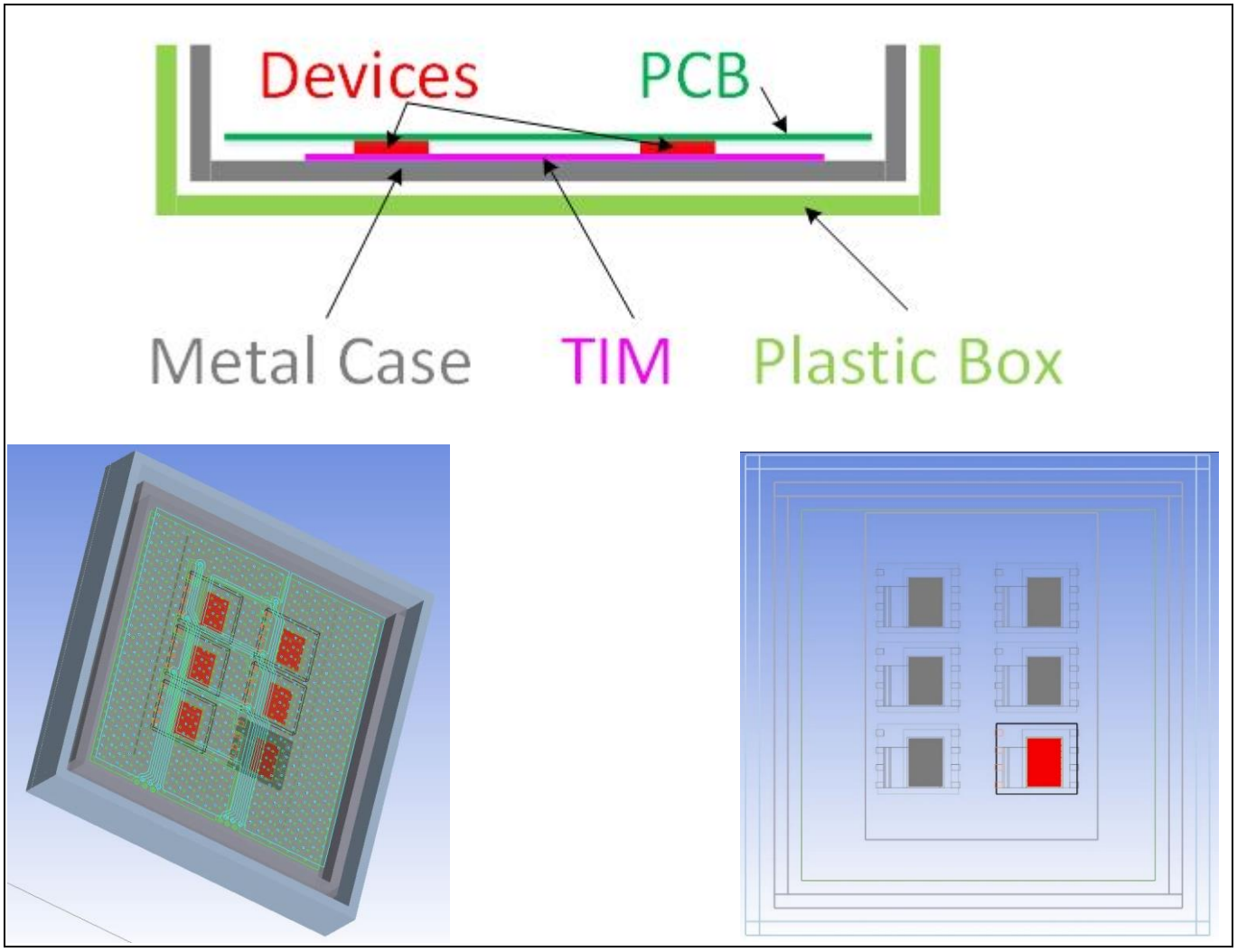


Figure 13 Simulation setup (top), 3D view (left) and top view (right)

Figure 13 shows the setup of the simulation; the figure on top is not to scale, and shows the overall system. The devices are mounted on the top layer, which is then flipped toward the bottom; therefore, the PCB faces the upper side of the system. Then the devices are thermally connected to the metal case through a thermal interface material (TIM; **Bergquist™** [5] with the following characteristics: 5 W/m-k; 1000 J/kg-k; 3600 kg/m^3). The metal case is then enveloped in the plastic case that normally surrounds the tool. In the case of dual-side cooled the TIM is placed on top of the clip; meanwhile in the bottom-side cooled there is the mold compound in between.

The picture at bottom left shows the 3D model with some transparency to show the location of the components. Meanwhile the picture at bottom right is a top view of the system, highlighting the source of the heat (the die in red) and some package details.

The main difference between this and the real application is that the upper part of the system is not closed but left open. The reason for this choice is to simplify the simulation.

Two kinds of simulations have been considered: static and dynamic. The reason for this approach is to highlight that sometimes the expected advantage does not happen as predicted in the product-level simulation.

All the simulations are done with an ambient temperature of 20°C and with gravity in the Z direction. The software used for the simulation is **ANSYS** Icepak™ 2019 R1 [6]. Since the goal of this application note is to discuss results, we will limit the description of the thermal simulation setup to the most important parts.

3.1.2.1 Static simulation

This paragraph shows the results and comparisons for static simulation between the dual-side cooled and bottom-side cooled. A load of 0.5 W is applied to each device indefinitely, for a total power dissipation of 3 W.

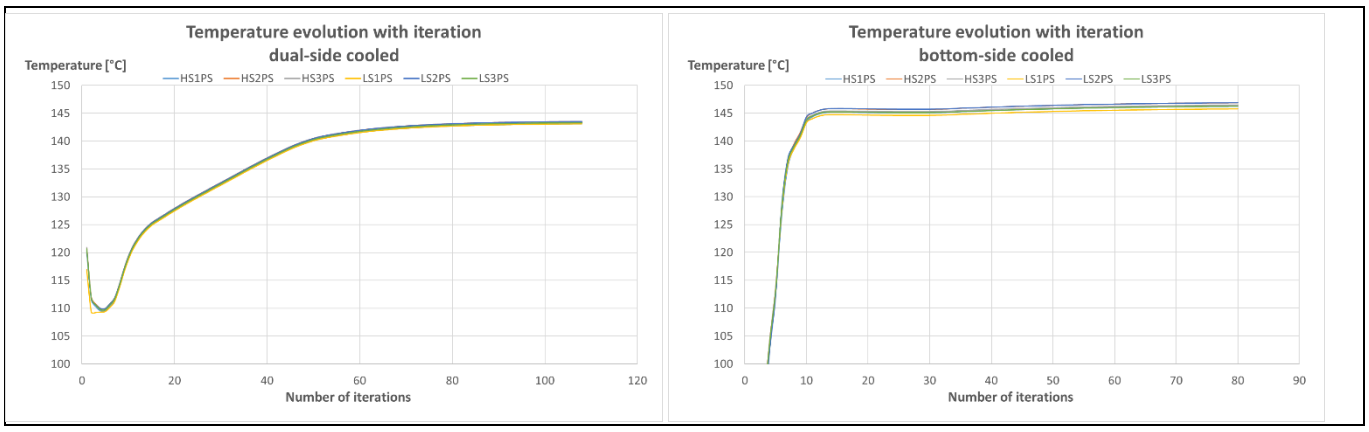


Figure 14 Temperature evolution for dual-side cooled left) and bottom-side cooled (right)

Figure 14 shows the temperature evolution for dual-side cooled and bottom-side cooled. It is important to remember that the X axis is not time but simply the number of iterations required by the software to reach a certain level of convergence.

Aside from the different evolution, there are two important factors to be highlighted: the first is the very small difference between the maximum temperature of the bottom-side cooled (143°C) and the maximum temperature of the bottom-side cooled (147°C). This can be explained by the fact that in this case, the overall thermal resistance is so high (roughly 40 K/W) that even improving the thermal resistance from junction to top using the dual-side cooled in the place of the bottom-side cooled doesn't lead to any significant advantage, as also demonstrated in the last part of paragraph **3.1.1**.

The second observation is again related to a small but significant tendency: the final temperatures of the devices are slightly more widely distributed for the bottom-side cooled compared to the dual-side cooled. This is an indication that the heatsink also helps to equalize the temperatures of the different devices, reducing the gradient between different devices and therefore reducing the risk of failure.

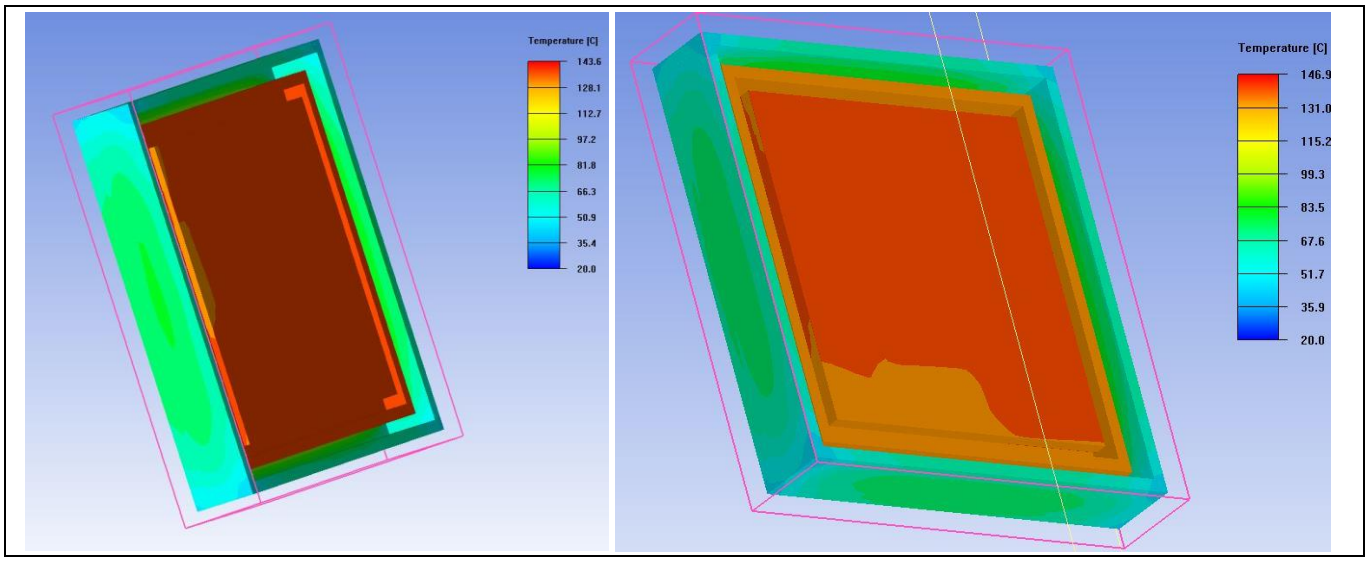


Figure 15 Temperature distribution of the dual-side cooled (left) and bottom-side cooled (right)

Figure 15 shows the temperature distribution for each device and the maximum junction temperature. The difference in terms of temperature is minimal; it is possible to see how in the case of the dual-side cooled the temperature of the metal case is more similar to the PCB and device temperature compared to the bottom-side cooled where the metal case clearly has a different color.

3.1.2.2 Dynamic simulation – load step

The same setup as used in the static simulation was used to run a load step dynamic simulation. In this case, a single pulse of 5 W was provided at the same time for the six devices, giving a total power dissipation of 30 W.

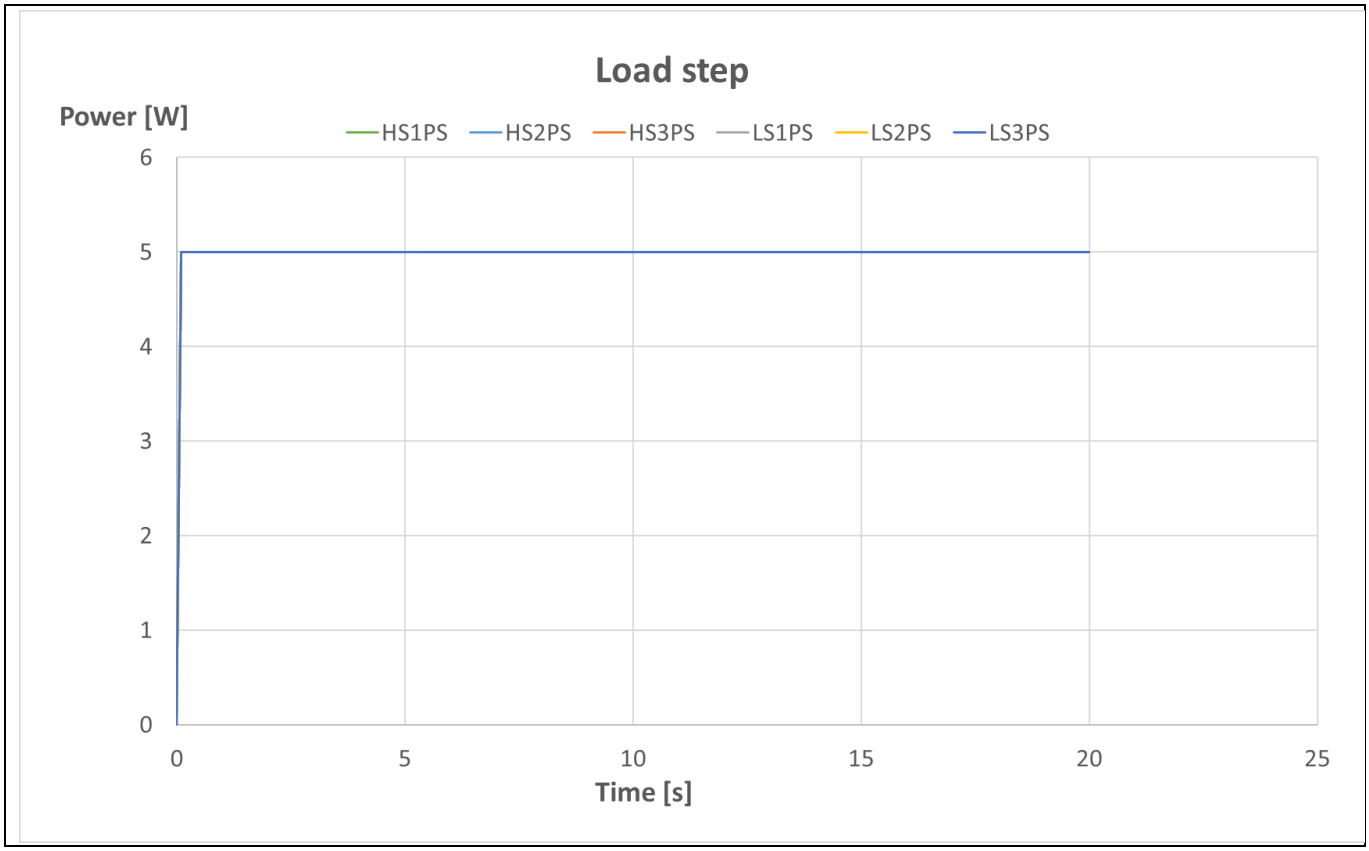


Figure 16 Power dissipation – load step

Figure 16 shows the load (heat) applied at the same time to all the six devices. The load is 5 W and has a rising edge of 0.1 s.

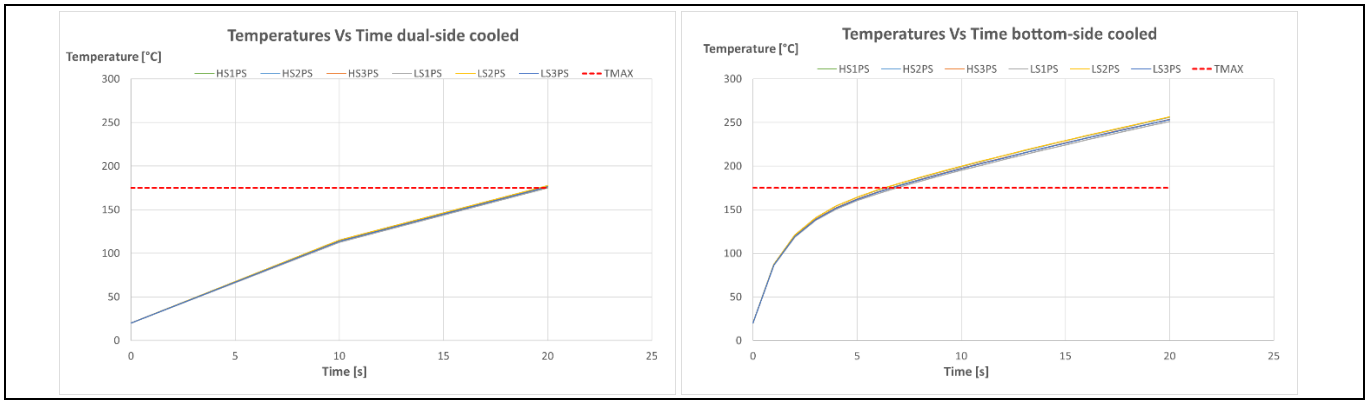


Figure 17 Temperature evolution for dual-side cooled (left) and bottom-side cooled (right)

Figure 17 show the temperature transient; on the left side there is the dual-side cooled and on the right side the bottom-side cooled. After 20 s, the dual-side cooled has slightly overcome the maximum allowed temperature of the device (175°C); meanwhile, in the case of the bottom-side cooled this happens after roughly 6 s.

3.1.2.3 Dynamic simulation – alternate load

Power tools using field-oriented control (FOC) are characterized by a sinusoidal current, due to the fact that in many cases the load is a motor. The sinusoidal current is used to set rotation speed and torque. Therefore the power losses related to conduction are a function of the sine current squared. In the end, the most application-relevant simulation is with a sinusoidal load. Since a sinusoidal waveform is computationally slightly more demanding for the simulation, an equivalent triangular shape has been used. **Figure 18** shows the comparison between the squared sinusoidal excitation and the triangular function.

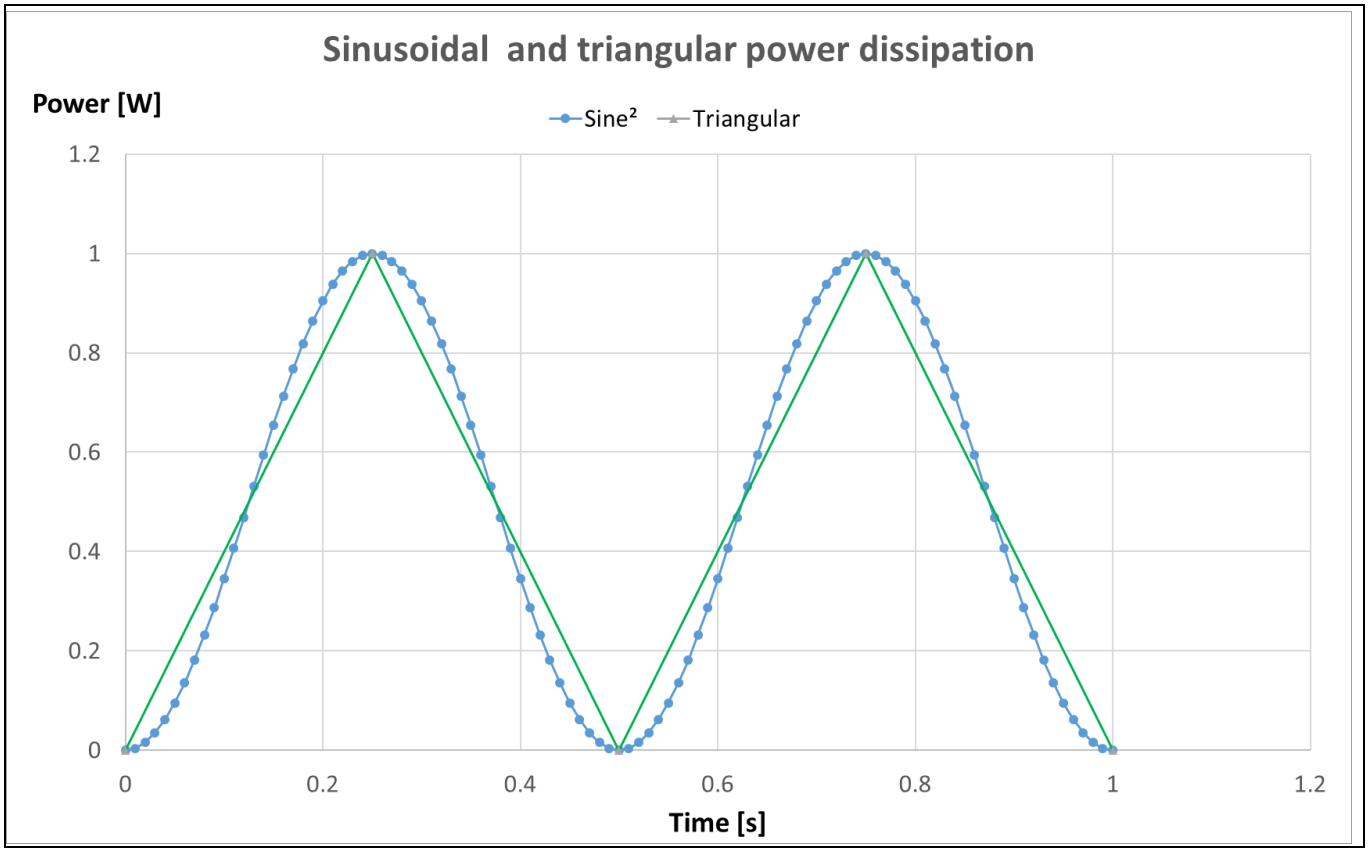


Figure 18 Approximation of the sin² function with a triangular function

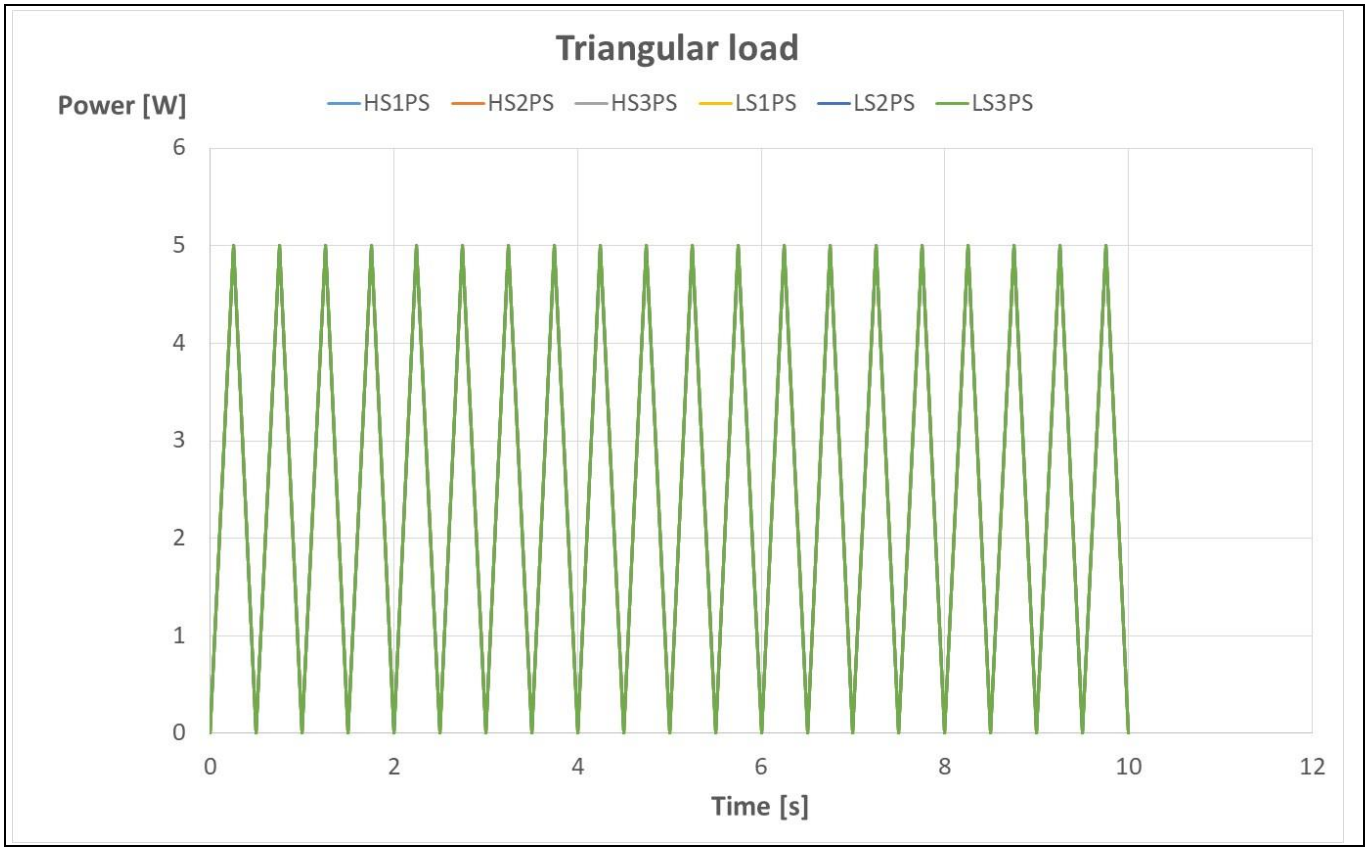


Figure 19 Power dissipation – triangular shape

Figure 19 shows the triangular-shaped power dissipation applied to the model. The maximum power is 5 W, the period is 0.5 s and the overall simulation time is 10 s.

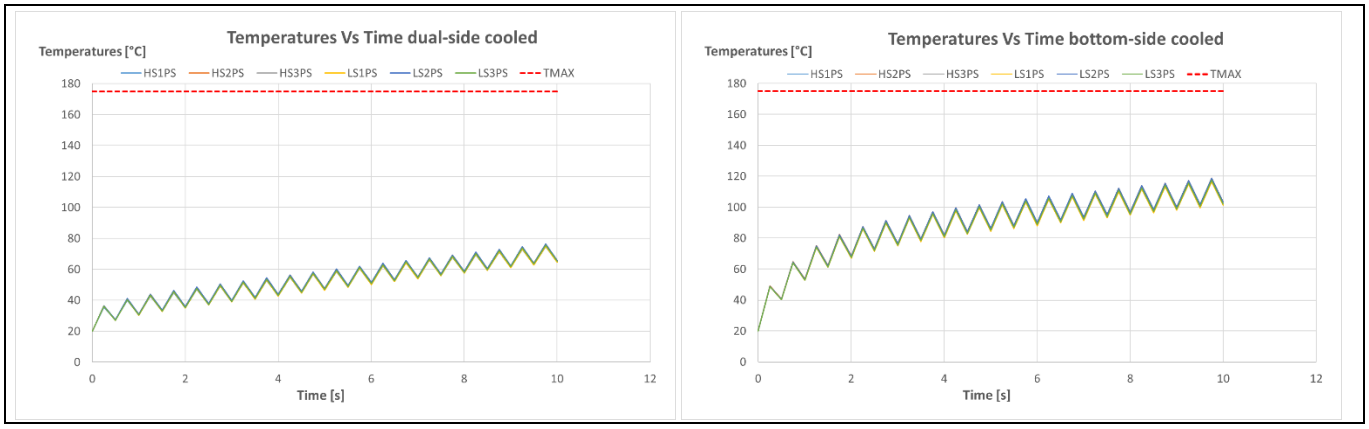


Figure 20 Temperature evolution for dual-side cooled (left) and bottom-side cooled (right)

Figure 20 shows the temperature evolution of the simulations for dual-side cooled (left) and bottom-side cooled (right). Neither of them have finished the transient yet, but it is evident how the dual-side cooled provides an advantage; in fact, for the same power dissipation the temperature after 10 s is roughly 70°C for the dual-side cooled and 110°C for the bottom-side cooled.

3.1.3 Application thermal performance – measurements

This paragraph will show the application measurements for different applications.

3.1.3.1 Telecom brick converter

The bottom-side cooled and dual-side cooled products from Infineon Technologies are qualified to industry level and are therefore suitable for telecom applications. For this particular test, the bottom-side cooled BSC040N10NS5 (bottom-side cooled) and the BSC040N10NS5SC (dual-side cooled) were compared.

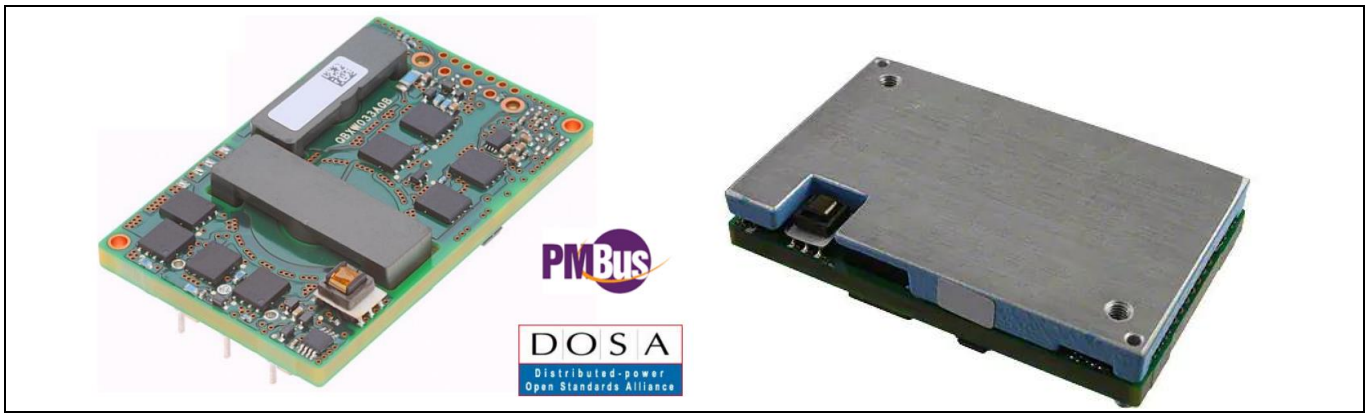


Figure 21 400 W brick converter used for the tests, with and without heatsink

Test conditions:

- A single device per leg was used during the testing instead of the original two devices per leg
- Fan speed is kept constant throughout the testing (5.4 V, 0.1 A)
- TIM of 0.9 K/W (placed only on synchronous devices)
- Burn-in time of 20 minutes at full load before taking measurements, and 1 minute burn-in time for each load change
- Load step of 3 A
- Temperature measured using a thermocouple (J-type), which was placed on the same reference point (source pin of SR1)

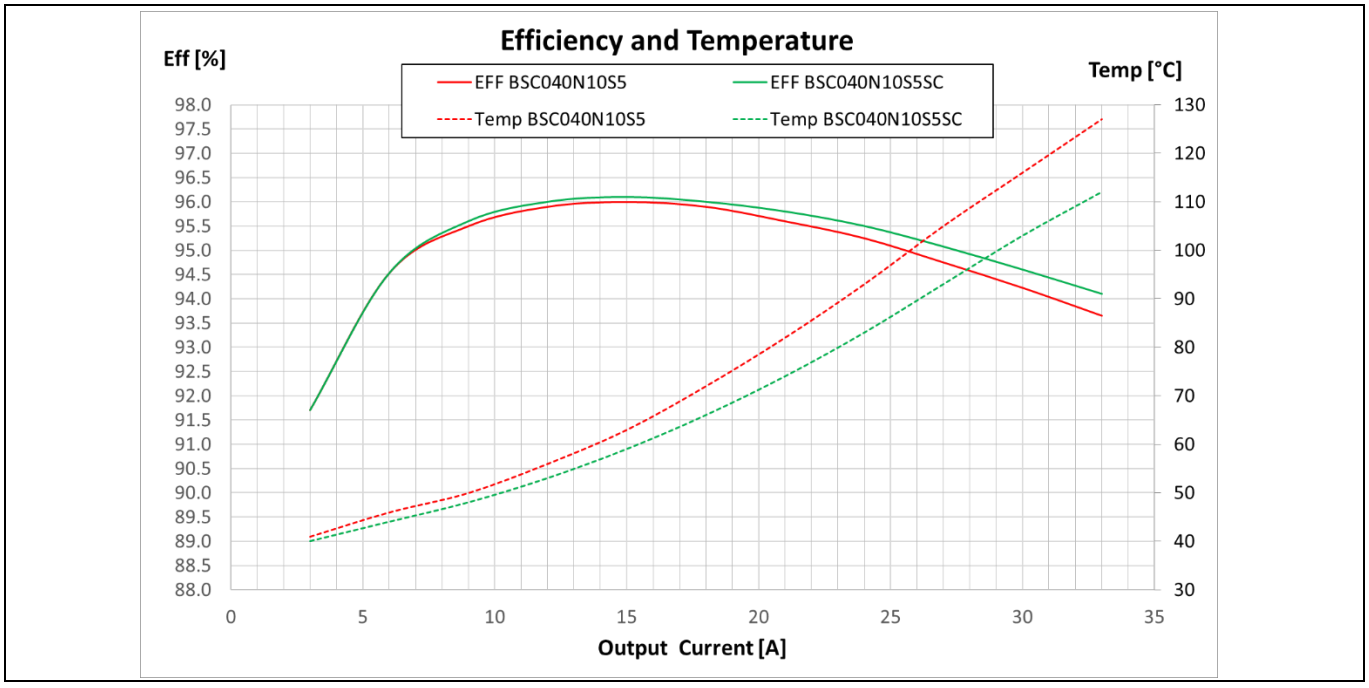


Figure 22 Efficiency and thermal comparison

Figure 22 shows the efficiency and the thermal comparison with an input voltage of 48 V. As shown, with the same $R_{DS(on)}$ class it is possible, due to the better connection to the heatsink, to achieve 0.4 percent higher efficiency and 15°C lower temperature on the board.

Another way to read the obtained results is to consider the increase of power density obtained with the dual-side cooled. If the maximum temperature of 110°C, for instance, is given, the dual-side cooled allows more output current, roughly 23 percent.

3.1.3.2 Switched mode power supply

This paragraph will show experimental results for the SMPS. In this case, the **EVAL_600W_12V_LLC_C7** [7] was used as the test platform. Some modifications were implemented to better suit the comparison between the dual-side cooled and the bottom-side cooled.

- The original synchronous rectifier (SR) device, BSC010N04LS, was replaced with the BSC016N06ST and BSC016N06NSSC.
- A heatsink was relocated on the top of the SR devices, separated by a thermal pad. This setup was performed for both bottom-side cooled and dual-side cooled
- Another fan was used, located on the bottom side of the board, which helped to cool down the heatsink for SR.
- Both fans were powered by an external DC source and not included in efficiency measurements.
- A thermocouple (J-type) was used to measure thermals and was put on a common point (the source pin of T6 and T10).
- The TIM thermal resistance was 0.9 K/W.

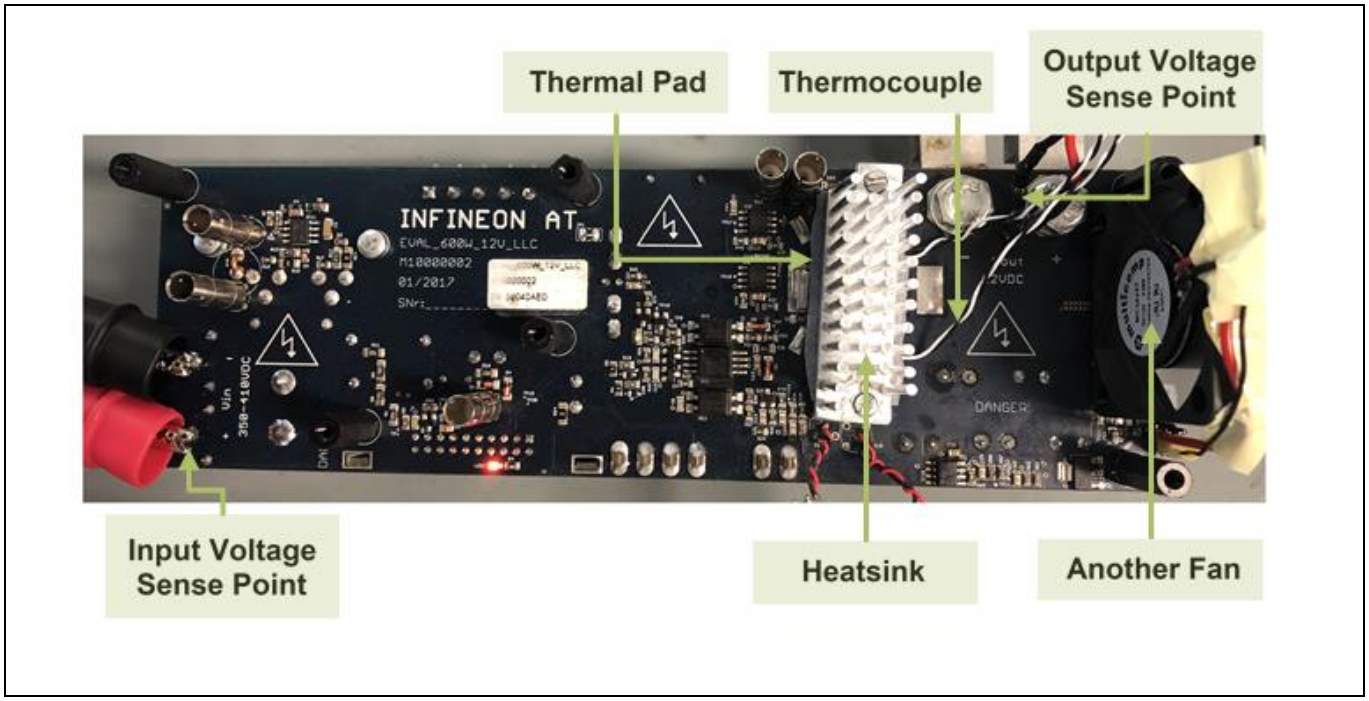


Figure 23 Test platform used for SMPS

Figure 23 shows the modified platform with the heatsink on top of the device.

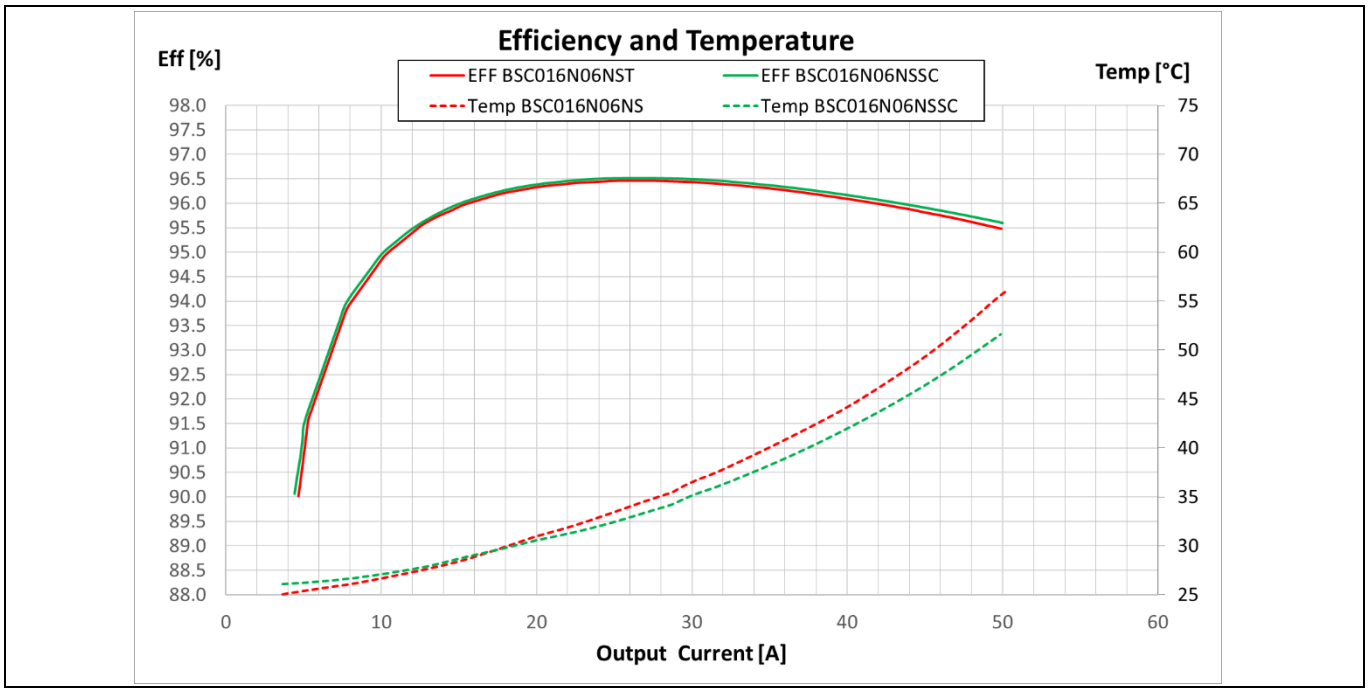


Figure 24 Efficiency and temperature comparison

In this case, the improvement is roughly 0.1 percent in terms of efficiency and roughly 4°C. For this application the increase in power density is in the range of 21 percent.

3.1.3.3 Power tools

This paragraph shows the results of the comparison between dual-side cooled and bottom-side cooled with different PCB setups. The test was a simple DC test where the current was increased gradually, and for each step the temperature equilibrium was awaited. The devices being compared were BSC014N06NS and BSC014N06NSSC. Still air was used in the test.

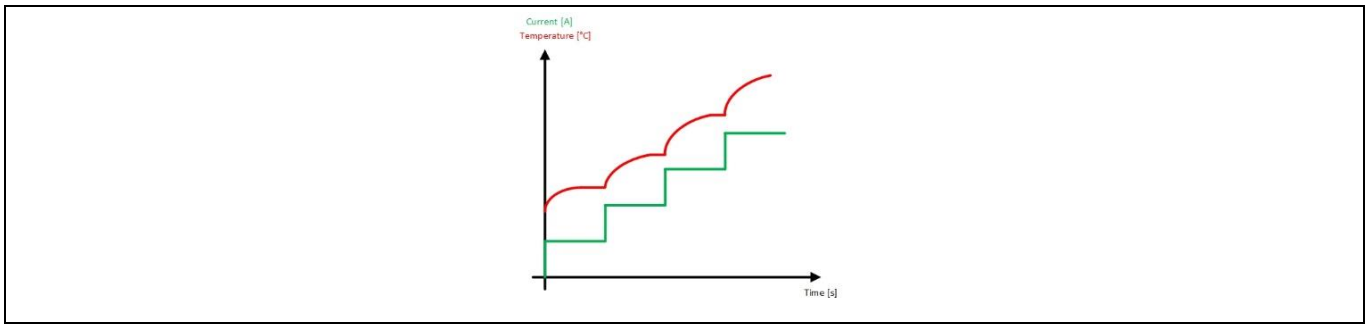


Figure 25 Visualization of the DC test current procedure

Table 5 PCB used for the DC tests

Board name	Size [mm]	Number of layers	Layer thickness [µm]
PCB_8L_280um_70um	76x76	8	280 top and bottom 70 internal layers
PCB_1L_70um	76x76	1	70
PCB_1L_35um	76x76	1	35

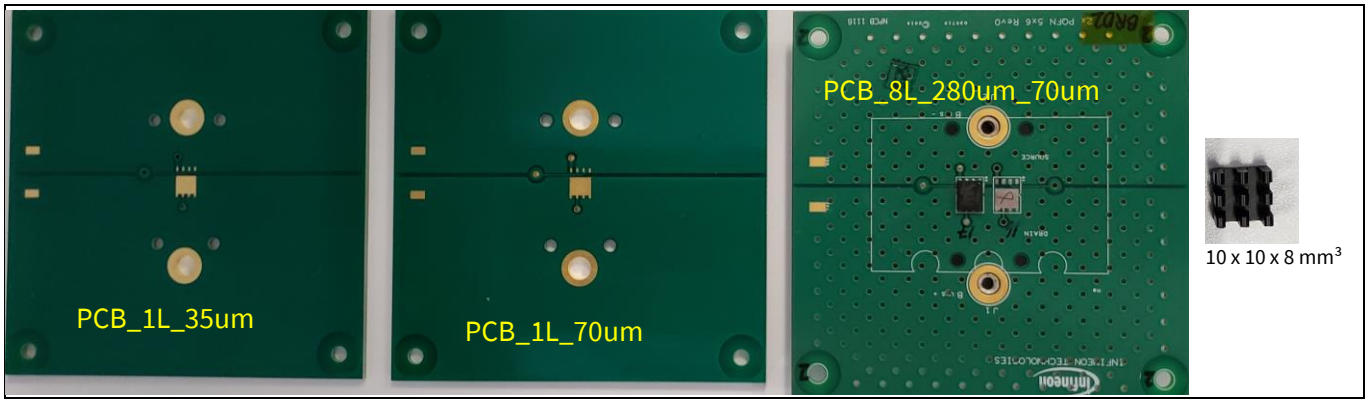


Figure 26 PCBs and heatsink used in the DC test

Figure 26 and **Table 5** show the characteristics of the PCB used for the DC test, and the heatsink, which is similar to the one used in the product-level simulation in paragraph **3.1.1**. The heatsink was attached to the top of the device with a thermal paste, and fixed to the PCB with screws.

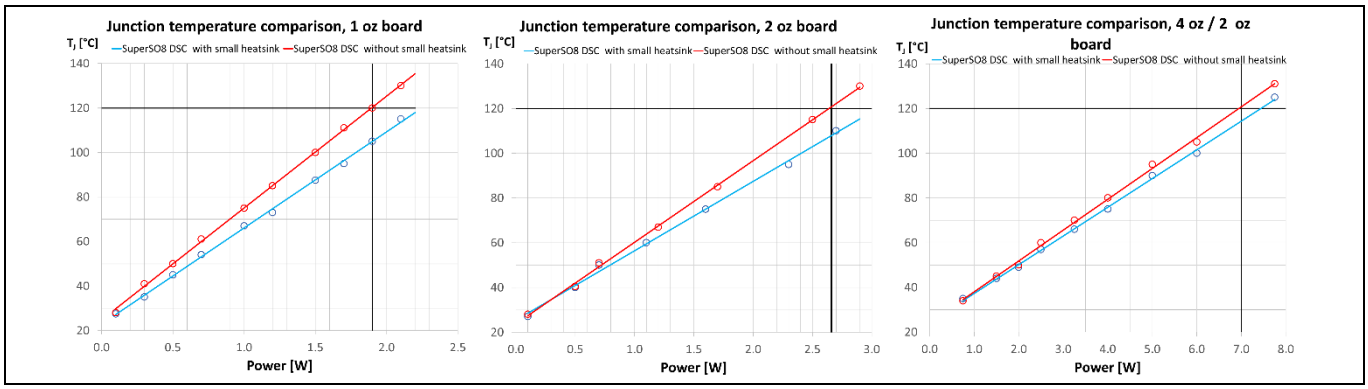


Figure 27 Thermal performance in the DC test with various PCB setups

Figure 27 shows the thermal performance of the dual-side cooled with and without heatsink; the picture on the right is the one with eight layers. The key assumption behind these measurements is that the dual-side cooled and the bottom-side cooled are behaving, from a thermal point of view, in a similar way as when they are mounted on the board and no heatsink is used. As shown, the improvement related to a small heatsink is normally negligible, roughly 10 percent from 7 W to 7.5 W higher power dissipation, when the board is very thick and equipped with a lot of copper; when the board has less copper the improvement is roughly 12 percent. In the last case, when the amount of copper used in the PCB is not extremely high, the improvement is more in the range of 20 percent.

3.1.4 Thermal performance – conclusion

The benefits of the dual-side cooled in terms of thermal improvements can be demonstrated in several ways: based on product-level or application-level measurements and simulations. The first approach, used in paragraph **3.1.1**, has the advantage of being very simple, not application specific and therefore very generic. However, this approach is sometimes too far away from the application conditions – because it employs PCBs that are too wide, or heatsinks that are too large, or it has only one heat source – to highlight a benefit that might not even be relevant for the application (the lower thermal resistance from junction to ambient).

The second approach, used in paragraph **3.1.2**, is severely limited by being too narrow and too specific to a given application; on the other hand, it has the advantage of showing that sometimes a solution provides completely unexpected benefits.

3.2 Mechanical performance

The improvements in thermal performance achieved with the dual-side cooled are very important, but they must come with no compromises. Exposing the clip of the device might mean it is considered less mechanically robust. In order to address this point two mechanical tests are performed: pressure and bending. The first is a device-level test, intended to measure the maximum pressure that can be applied to the device before a destructive degradation is observed. The second test, bending, is a secondary mechanical test, since it is not only related to the device itself but also to the attachment of the device to the PCB. [7] provides some indications of the mechanical performance of a bottom-side cooled as reference.

3.2.1 Compression test

The compression test is to measure the amount of force that can be placed on the device, for instance during the mounting phase of a heatsink, before the device has electrical failures. The pressure is then cycled a certain number of times, from zero to a maximum. The speed of the pressure cycling is also a parameter of the test. In some cases, the pressure can return to zero, while in other cases, it goes back to a pre-determined value. Furthermore, the maximum force is held at the final step or every cycle for 5 s. The number of samples used in this test is 10.

The reason for the different tests is to find out if there is any weak point in the mechanical structure, with different kinds of loads.

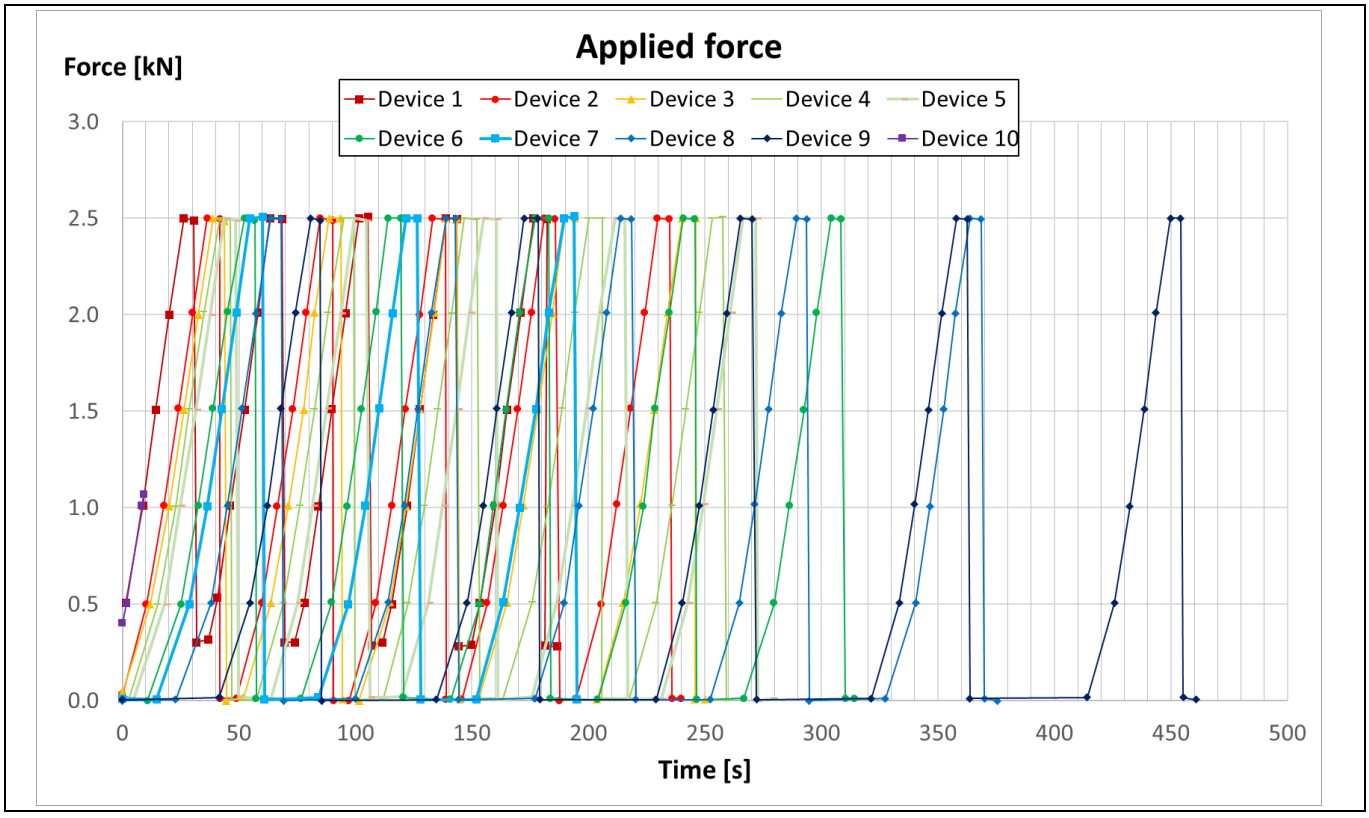


Figure 28 Pressure test – different test patterns

In this case, the maximum force applied is 2.5 kN and the agreed number of cycles is five.

Table 6 Summary results for pressure test

Device	Cycles	F_{max} [N]	Comment
1	5	2500	
2	1	1070	Electrical failure at 1 kN at the first cycle
3	5	2500	
4	5	2500	
5	5	2500	
6	5	2500	
7	5	2500	
8	5	2500	
9	3	2500	Electrical failure at 2.5 kN at the third cycle
10	5	2500	

The values obtained are in the same range as for the bottom-side cooled device. As the experiments show, the dual-side cooled can be considered as robust as the bottom-side cooled. In fact, the tests were run with a pressure that is far beyond the normal pressure used for heatsink attachment. To give a rough understanding of the numbers employed in the experiment, 2000 N is the rough equivalent of 200 kg, and this mass should be placed in the small area of 30 mm^2.

For the failing devices, there were two electrical failures, but no mechanical failure was visible.

3.2.2 Bending test

The bending test is part of the so-called “second-level tests”, which are not related to the device alone (such as the pressure test), but they tend to test the relation between the device and the supporting structure, like soldering on the PCB. The test has the purpose of proving the mechanical strength of the soldering junction between the device and PCB when a heatsink is mounted, and during the mounting the PCB could bend.

In this case, the test is conducted as follows: from a starting flat condition, the PCB is bent through an applied force, until a maximum bending factor is reached. The test is cycled with an increasing maximum bending factor. At the end of the cycle the bending is reduced to the initial value. Unlike in the previous test, the final bending state is not held. Also for this test, 10 samples are used.

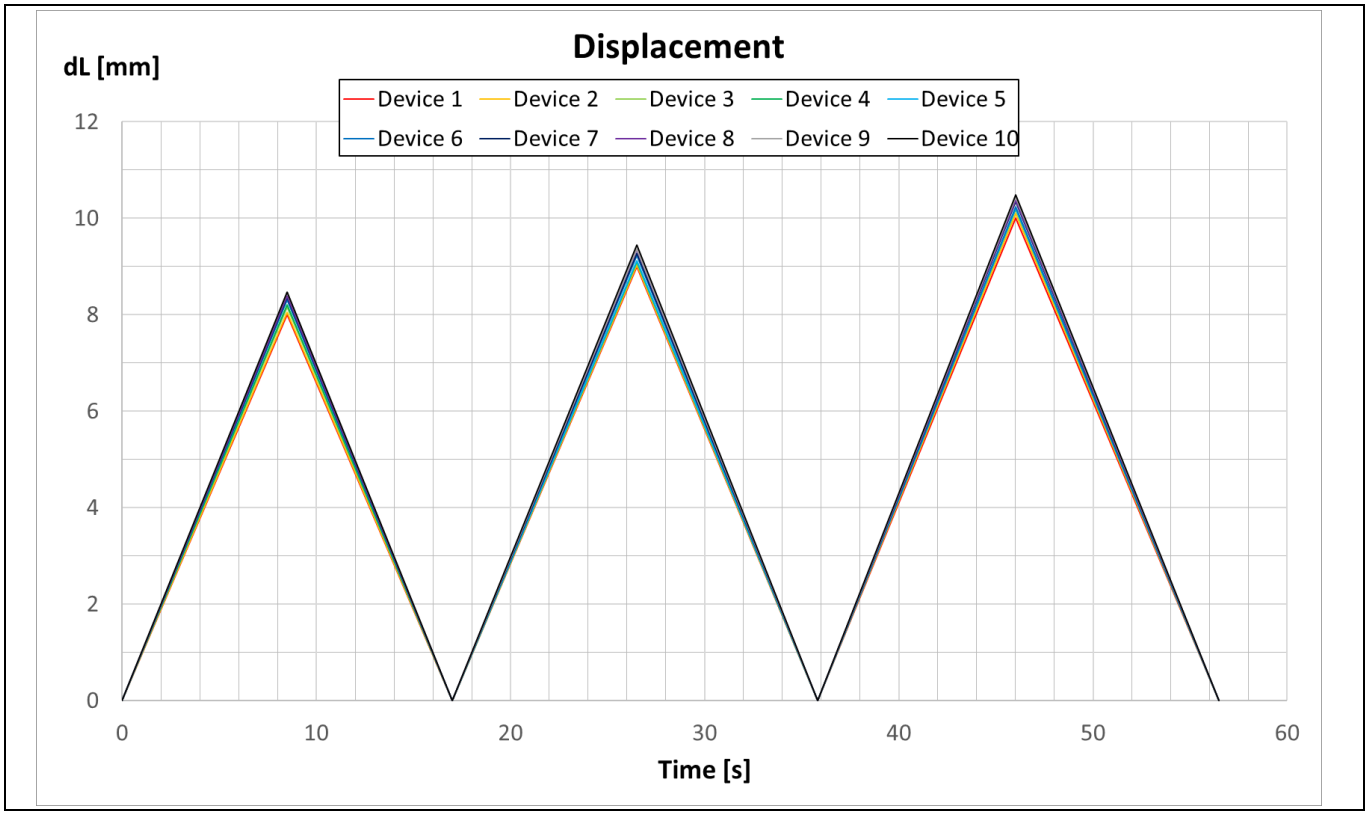


Figure 29 Bending test – pattern

Table 7

Device	Cycles	$F_{max.}$ [N]	dL [mm]	Comment
1	3	156	10	
2	3	158	10	
3	3	157	10	
4	3	156	10	Electrical failure after three cycles from low to high
5	3	159	10	Electrical failure after three cycles from low to high
6	3	154	10	
7	3	159	10	
8	3	158	10	
9	2	145	9	Electrical failure after two cycles from low to high
10	3	154	10	

As for the pressure testing, the amount of stress applied to the part is very high; in fact, it is very unlikely that the bending during the mounting of the heatsink would reach such a level of 10 mm. Furthermore, it is important to notice that an electrical failure doesn't mean that the device is failing, but simply that the soldering between the device and the PCB was broken.

The values obtained are similar to the bottom-side cooled device.

3.2.3 Mechanical simulations

This paragraph will offer a mechanical comparison between the dual-side cooled and bottom-side cooled with the help of simulations. The idea is to replicate a possible application condition, as for the thermal simulation in the previous chapter, and to investigate the robustness of the dual-side cooled device in comparison with the bottom-side cooled during a mechanical load, which would represent the mounting process of a heatsink.

3.2.4 Mechanical simulation – setup

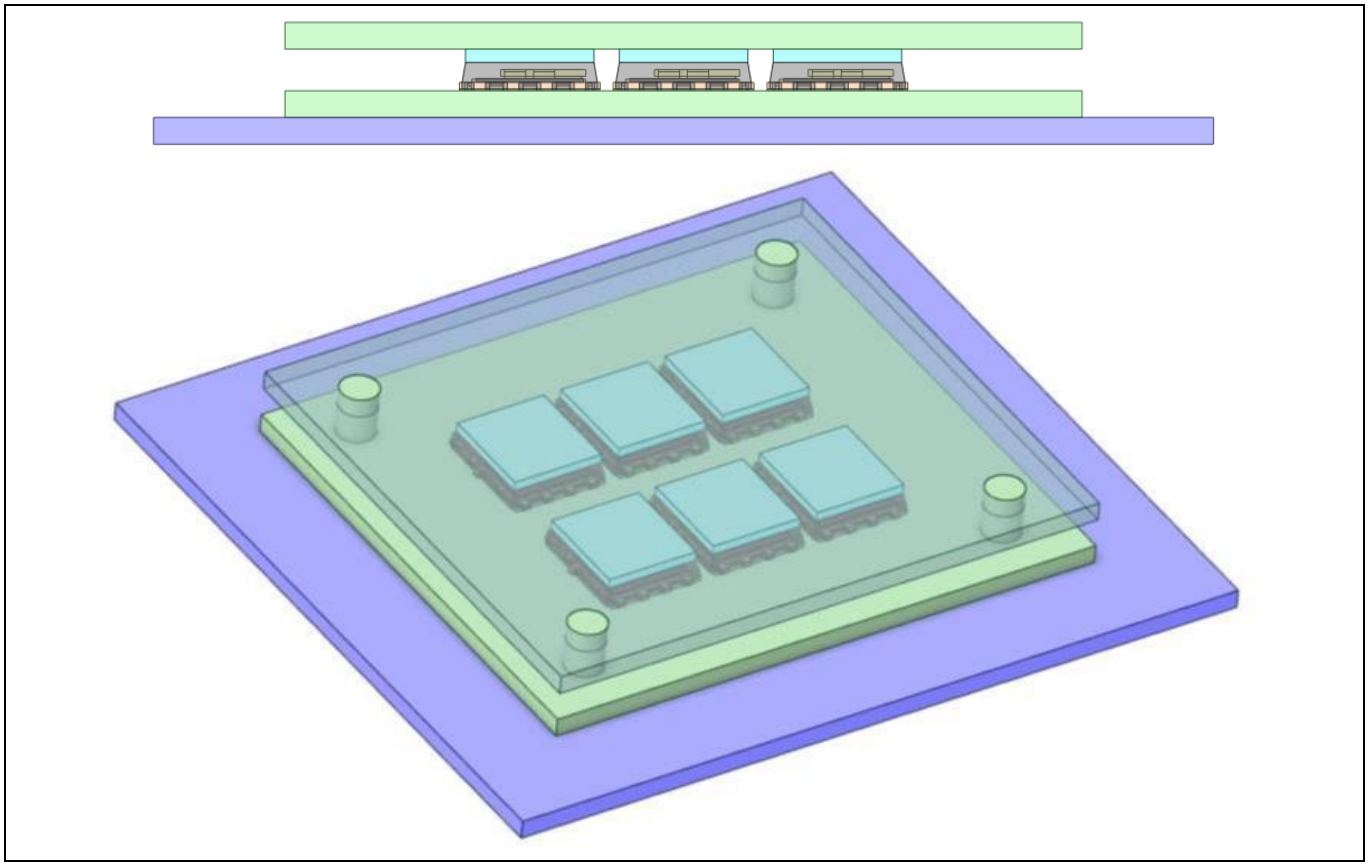


Figure 30 Test setup for mechanical simulation (bottom-side cooled)

The setup chosen for the mechanical simulation is similar to the one used in the thermal simulation. **Figure 30** shows the version for the bottom-side cooled; the dual-side cooled uses the same configuration. The setup consists of:

- a simple PCB with 1.6 mm total height, with two layers of copper of 70 µm
- six devices
- semi-soft TIM with 500 µm initial thickness
- an aluminum-based heatsink of 1 mm height, fixed with four screws at the corners.

In this case, for the simulation, a plastic model for the heatsink is used.

The structural loading is applied to the screws, to simulate bending in the heatsink once the screws are tightened.

3.2.5 Mechanical simulation – results

The primary result of the applied force, during the tightening process of the screws, is the deformation of the heatsink and the PCB. Due to the highly symmetrical structure, the simulation is limited to half of it.

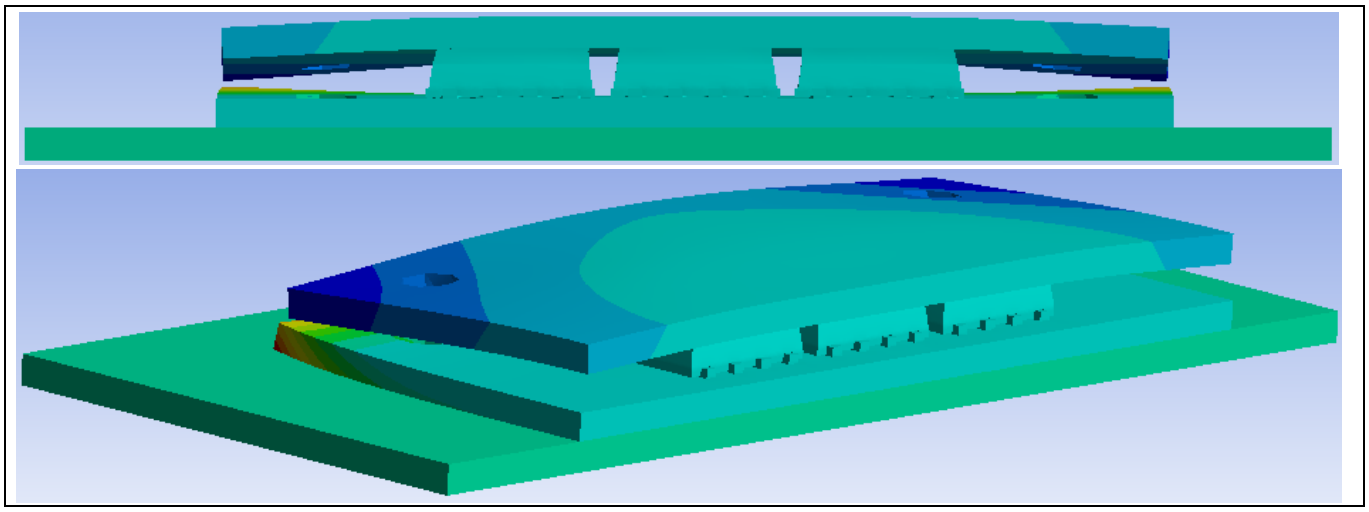


Figure 31 Deformation happening after application of the mechanical load

Figure 31 shows the deformation of the PCB and the heatsink after applying the mechanical load related to the tightening process of the screw. The picture shows an extreme case that should never be achieved in the real application. The purpose is to show what happens to the silicon dies inside the device once this extremely high force is applied, but in any case, a force should never reach a level that generates a deformation of the heatsink and/or the PCB.

Once the heatsink and the PCB are deformed, the silicon dies also suffer the same deformation. The direction of the deformation will depend on which one of the two structures is less flexible. In the actual case the softer material is the FR4 of the PCB, therefore the silicon dies will bend according to the heatsink bending direction. **Figure 32** shows the effect of the heatsink deformation on the silicon die; the same deformation present in the heatsink is also visible in the silicon die. The central silicon die is more affected by this deformation compared to the lateral silicon dies.

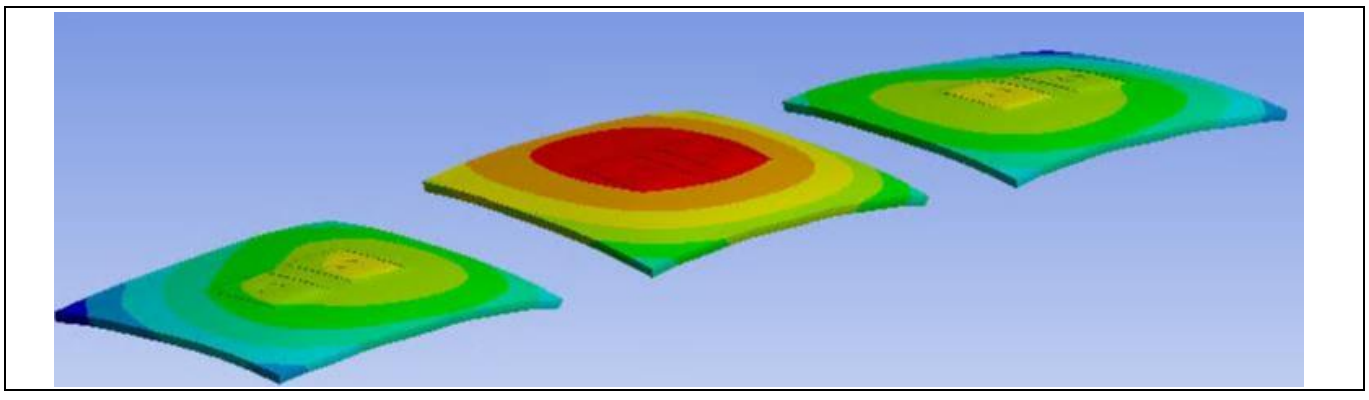


Figure 32 Example of deformation of the silicon dies

The deformation of the silicon dies is then responsible for possible fractures in the silicon die structure, which might lead to component destruction or decrease the lifetime of the device due to the weakening of those

structures; therefore the silicon-level mechanical stress is essential as a term of comparison between the two different solutions,: dual-side cooled and bottom-side cooled.

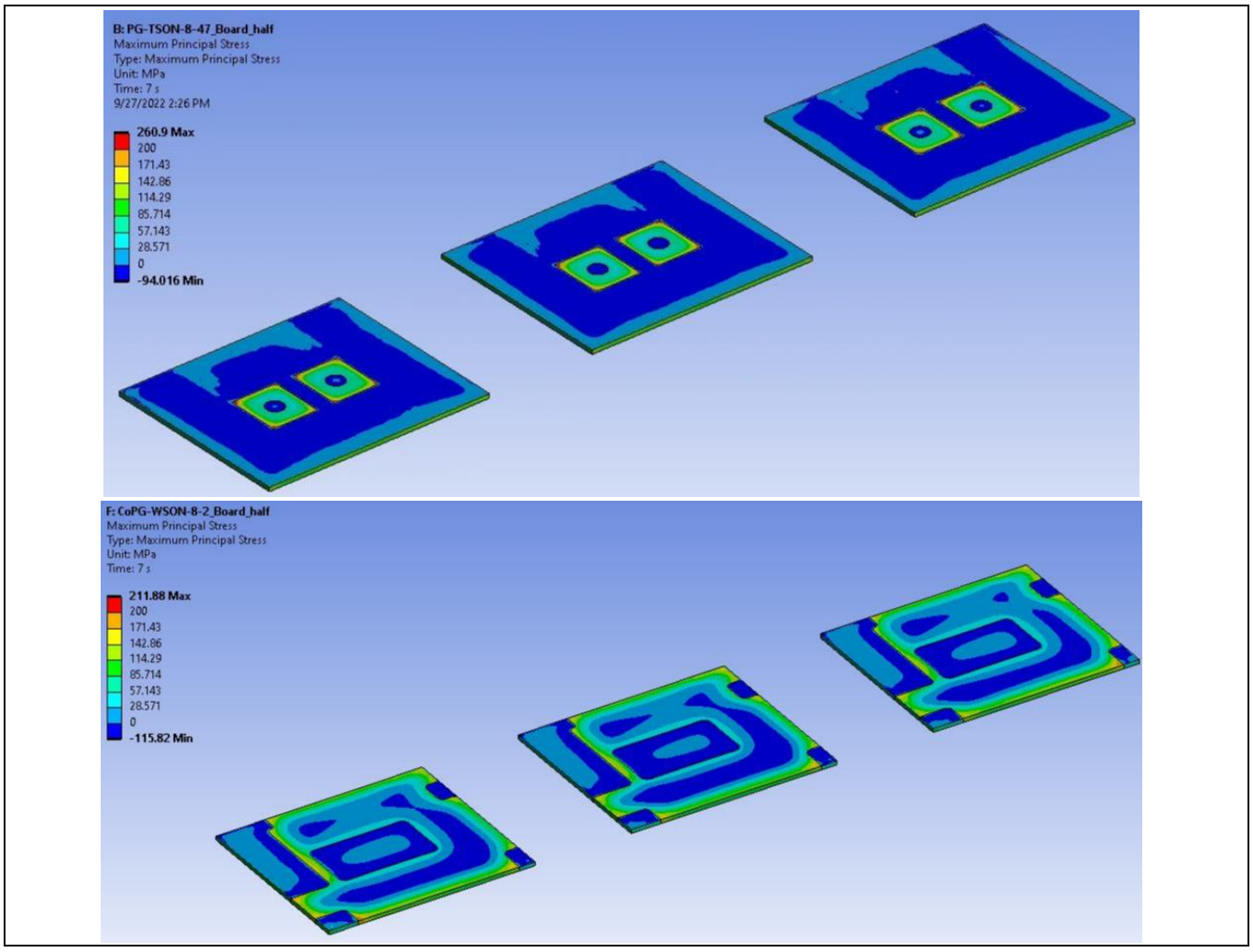


Figure 33 Stress comparison for bottom-side cooled (top) and dual-side cooled (bottom) – system level

Figure 33 offers an overview of the comparison between the stress on the bottom-side cooled and the dual-side cooled devices with the different dies. Aside from the slightly different maximum stress, there are some common aspects. The first is that the stress is at a maximum around the attachment of the clip to the die. The second is that the stress is very low in the area of the silicon dies covered with mold compound.

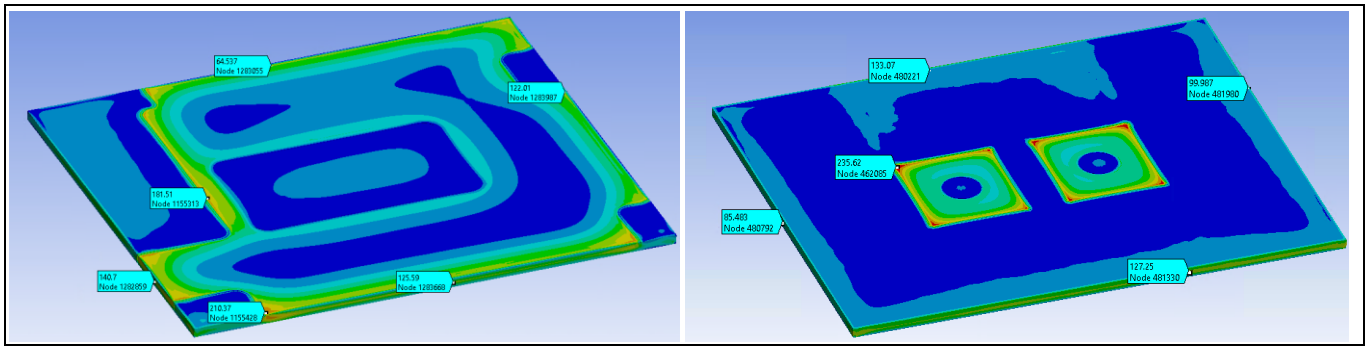


Figure 34 Stress comparison – silicon die level

Figure 34 shows the stress on the die level in more detail. As shown, the stress level is even smaller for the dual-side cooled device compared to the bottom-side cooled device based on the fact that the clip is attached on a larger area of the silicon and therefore has more distributed stress. Furthermore, the stress at the border region, normally an area subject to less damage, is at a similar level.

3.2.6 Mechanical performance – conclusions

For both the pressure and bending tests, the values applied are far beyond to the stress normally considered. The results obtained for dual-side cooled are in line with the known values for bottom-side cooled. Also, from a simulation point of view, it is possible to see that the dual-side cooled device is as robust as the bottom-side cooled. The dual-side cooled device can be considered as solid as bottom-side cooled, and therefore can be considered as a replacement in an existing board.

3.3 Maximum current

As described in [9], the maximum current of the device is calculated theoretically, by a formula:

$$I_D(T_C) = \sqrt{\frac{(T_J - T_C)/Rth_{JC}}{R_{DS(on),T_{JMax}}}}$$

As shown, this implies that the bottom side of the device (bottom-side cooled) is kept at a maximum temperature of 25°C.

3.3.1 Maximum current – calculation options

In order to determine the maximum current for dual-side cooled products, there are different approaches. This is related to the fact that once the top surface of the device becomes thermally available, in theory, one could also fix the top-side temperature to a given value.

The first approach is to apply the same definition of bottom-side cooled, and therefore fix only the bottom side of the package to 25°C. This will lead to the same maximum current as for the bottom-side cooled. This is the simplest approach, and it is the one Infineon Technologies has chosen, to simplify adoption of the dual-side cooled as a replacement for the bottom-side cooled with the same $R_{DS(on)}$.

A second possible approach is to apply the same methodology used for bottom-side cooled to the dual-side cooled, with the difference of setting both top and bottom at the temperature of 25°C. In this case, the theoretical maximum current would be roughly 40 to 50 percent higher. This is related to the values of $R_{thJC(top)}$ and $R_{thJC(bot)}$; since the values of the thermal resistances, for best-in-class devices, are similar between top and bottom, this would lead to an overall thermal resistance, which would be half compared to the bottom-side cooled and therefore an increase of 40 percent of the current.

Table 8 Comparison – maximum current between bottom-side cooled and dual-side cooled

5x6 PQFN bottom-side cooled	I_D [A] Bottom case fixed to 25°C	5x6 PQFN dual-side cooled	I_D [A] Top and bottom case fixed to 25°C
BSC007N04LS6	381	BSC007N04LS6SC	555
X	301	BSC009N04LSSC	430
BSC014N06NST	257	BSC014N06NSSC	380
BSC016N06NST	234	BSC016N06NSSC	334
BSC028N06NST	137	BSC028N06NSSC	197
X	202	BSC023N08NS5SC	293
X	144	BSC033N08NS5SC	217
X		BSC030N10NS5SC	
BSC040N10NS5	136	BSC040N10NS5SC	197
BSC070N10NS5	80	BSC070N10NS5SC	115
BSC093N15NS5	87	BSC093N15NS5SC	130
BSC110N15NS5	76	BSC110N15NS5SC	117
BSC160N15NS5	56	BSC160N15NS5SC	86

Table 8 shows the increase of the maximum current according to the theoretical calculation based on the top side fixed to 25°C.

A third possible approach is to use a more application-oriented calculation based on the thermal resistance of a certain PCB and a certain heatsink. This method offers a more realistic increase in current but is strongly dependent on the conditions. The idea behind this solution is similar to the one in paragraph 3.1.1.

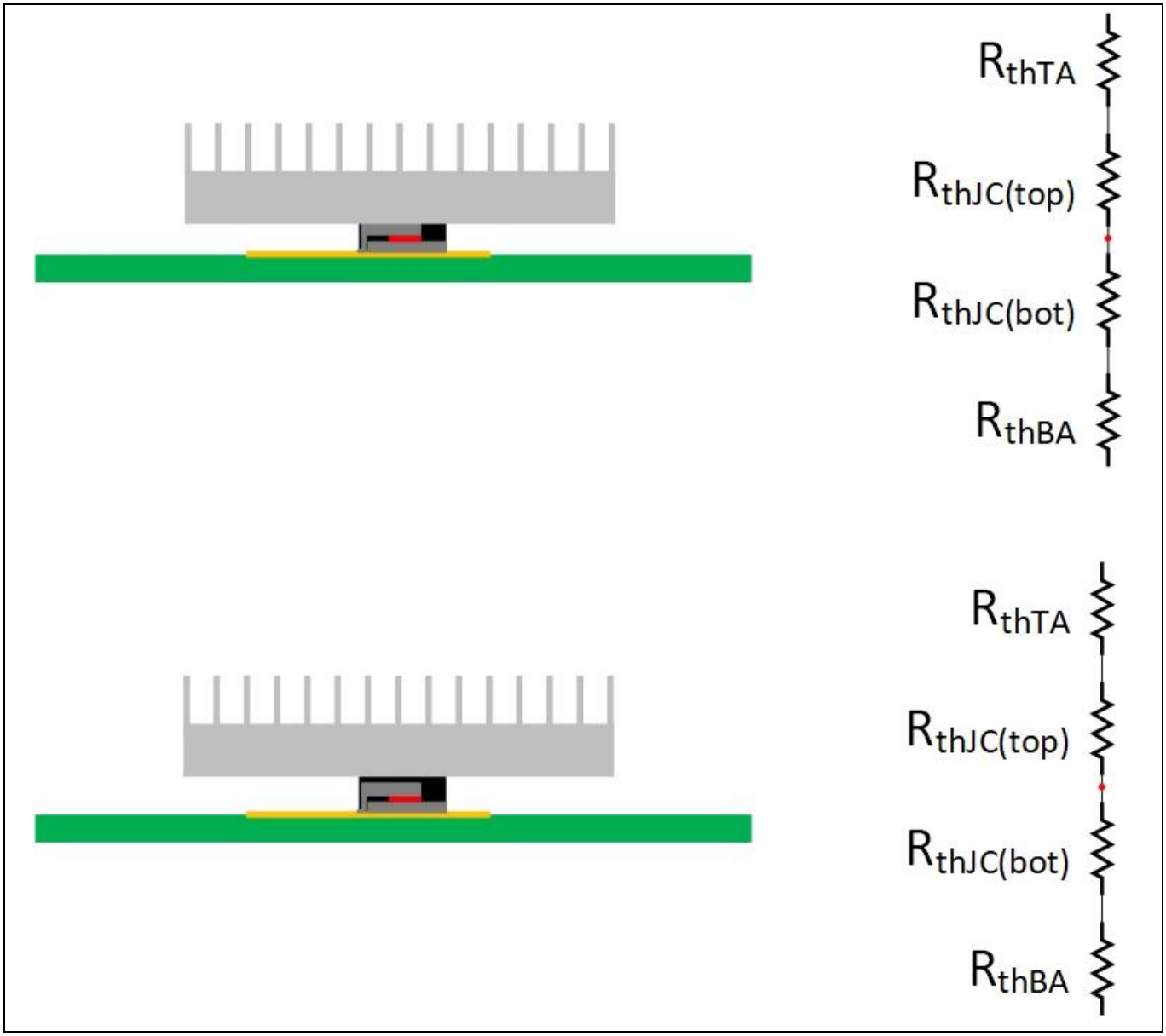


Figure 35 Maximum current calculation with heatsink – simplified model of dual-side cooled (top) and bottom-side cooled (bottom)

Figure 35 shows a simplified approach for calculating the maximum current for a dual-side cooled and bottom-side cooled considering a heatsink. The thermal resistance with a PCB is already provided in the datasheet as R_{thJA}, and for a PQFN 5x6 is normally in the range of 50 K/W. The assumption behind the approach adopted is that adding a heatsink will change only the thermal resistance from top to ambient. Therefore, the parallel of the top thermal resistance and the bottom thermal resistance, as in the following formula, will give the overall resistance.

$$R_{th} = \frac{\left(R_{thJC(top)} + R_{thTA}\right) * \left(R_{thJC(bot)} + R_{thBA}\right)}{\left(R_{thJC(top)} + R_{thTA}\right) + \left(R_{thJC(bot)} + R_{thBA}\right)}$$

As shown in the formula, the main difference will be between a bottom-side cooled and the dual-side cooled on the top path, where the low thermal resistance from junction to top will provide a benefit.

A relatively small heatsink (something like 15 mm x 15 mm x 8 mm) has a thermal resistance in the range of 20 K/W. Therefore, the expected improvement in terms of maximum current is in the range of 20 percent.

Table 9 Comparison – maximum current between bottom-side cooled and dual-side cooled with 20 K/W heatsink

5x6 PQFN bottom-side cooled	I_D [A] With heatsink	5x6 PQFN dual-side cooled	I_D [A] With heatsink
BSC007N04LS6	72	BSC007N04LS6SC	89
X	X	BSC009N04LSSC	X
BSC014N06NST	47	BSC014N06NSSC	57
BSC016N06NST	47	BSC016N06NSSC	57
BSC028N06NST	36	BSC028N06NSSC	44
X	X	BSC023N08NS5SC	X
X	X	BSC033N08NS5SC	X
X	X	BSC030N10NS5SC	X
BSC040N10NS5	27	BSC040N10NS5SC	33
BSC070N10NS5	21	BSC070N10NS5SC	26

Table 9 shows the maximum current comparison between bottom-side cooled with heatsink and dual-side cooled with heatsink; roughly 20 percent higher current for dual-side cooled.

3.3.2 Maximum current – conclusions

Many different conditions influence the maximum current. Due to this dependency it is not possible to uniquely quantify the maximum current increase of the product. Nevertheless, it is also reasonable to say that a range of improvements between 20 and 50 percent can be achieved in terms of maximum current when a dual-side cooled replaces the bottom-side cooled.

4 Top-side cooling – best practice

To completely appreciate the benefits of a dual-side cooled a series of precautions must be taken, especially in mounting the heatsink. This paragraph covers a few important pitfalls, but the complete list might require a longer description available in more specialist literature.

4.1 Dual-side cooling structure

In order to use the dual side cooling effectively, it is necessary to pay particular attention to the composition of the cooling concept.

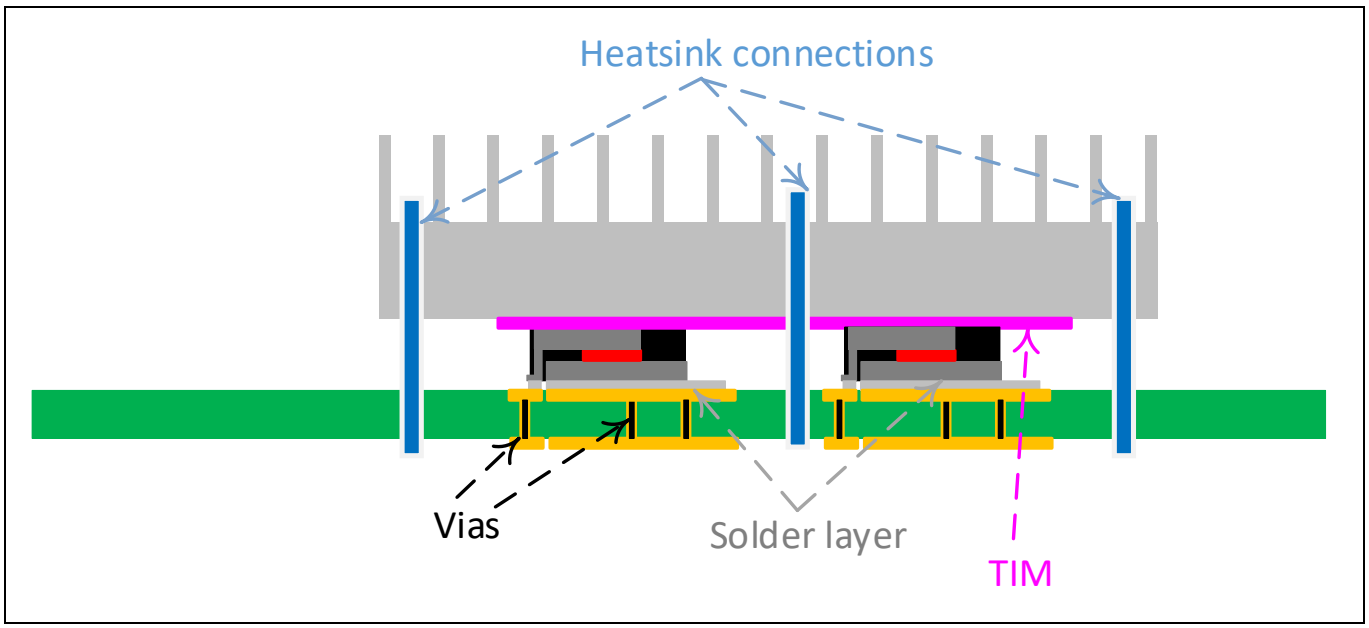


Figure 36 Duals Side Cooled concept with three-point heatsink connection

Figure 36 shows a simplified version of the dual side cooling essential elements:

- Soldering of the package on the PCB
- Vias structure
- TIM
- Heatsink connection

4.2 Soldering of the package on the PCB

General recommendations for PQFN 5x6 soldering are included in [8]; what is important to highlight beyond those documents, which is partially addressed in [10], is the risk of vertical tilting of the package (tombstoning), which is normally defined by the tilting angle. **Figure 37** gives an idea of this issue (extremely exaggerated).

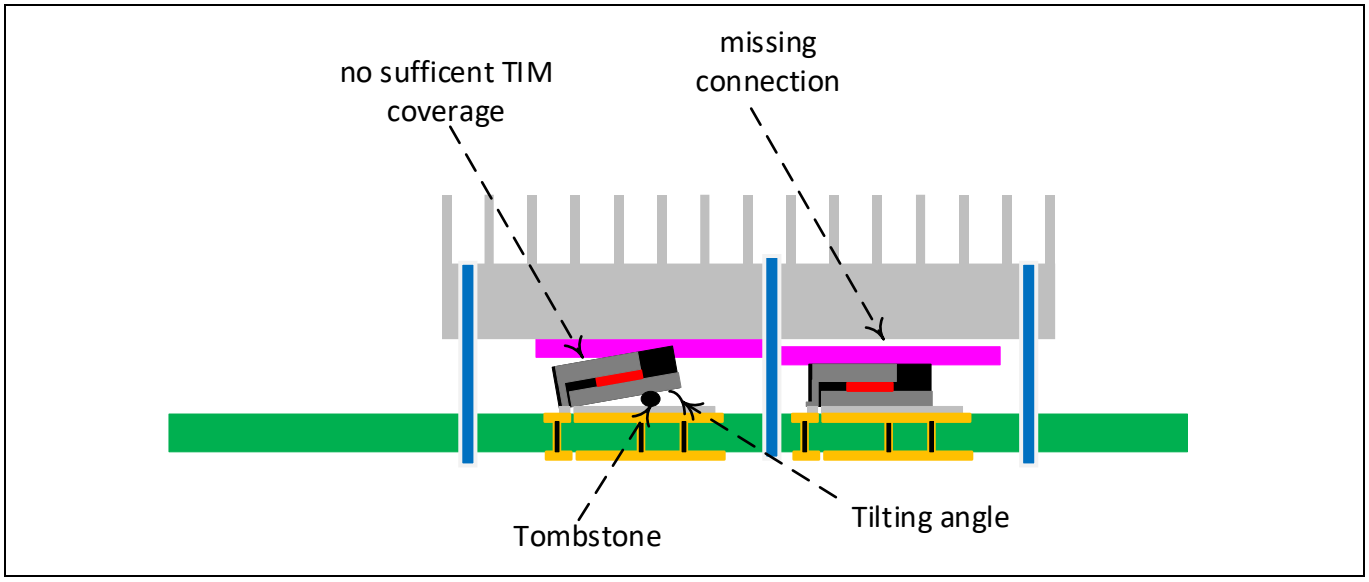


Figure 37 Effects of tombstoning

The root causes of this can be multiple, from layout to soldering process impurities. Normally this effect can be ignored, because even if bottom-side cooled power MOSFETs operating in the same mode have some tilting, in most cases this won't affect performance.

However, in the case of a dual-side cooled using a top heatsink, excessive tilting can increase the thermal resistance significantly for the affected device, leading to hot spots and possible reduction of lifetime.

4.3 Vias structure

Placing vias under the pad is a very common way of using the PCB as a heatsink and decreasing the thermal resistance of the device. The optimal number of vias is a separate matter from the production of a PCB, which requires focused investigation into the production process.

It is important to highlight that many tests and simulations have shown that increasing the number of vias above a certain number does not lead to a proportional decrease in thermal resistance.

Furthermore, if the vias have too large a diameter, the risk of capillary effects on the solder is increased. In this way the solder can flow through the vias and leave voids in the pad, increasing the thermal resistance.

4.4 Thermal interface material

In order to compensate for the tombstone effect, the difference in the height of similar components and the roughness of the top composite surface, in many cases a buffer layer is introduced between the top side of the package and the bottom side of the heatsink; this layer is filled with so-called thermal interface material (TIM). As reported widely in [11], the TIM can be formed by different materials in different states (e.g., grease, soft compound), but the main purposes of this layer are:

- To equalize different heights and compensate for tilting/tombstoning
- To fill in any roughness on the top side of the components
- To provide sufficient electrical isolation, but good thermal connection

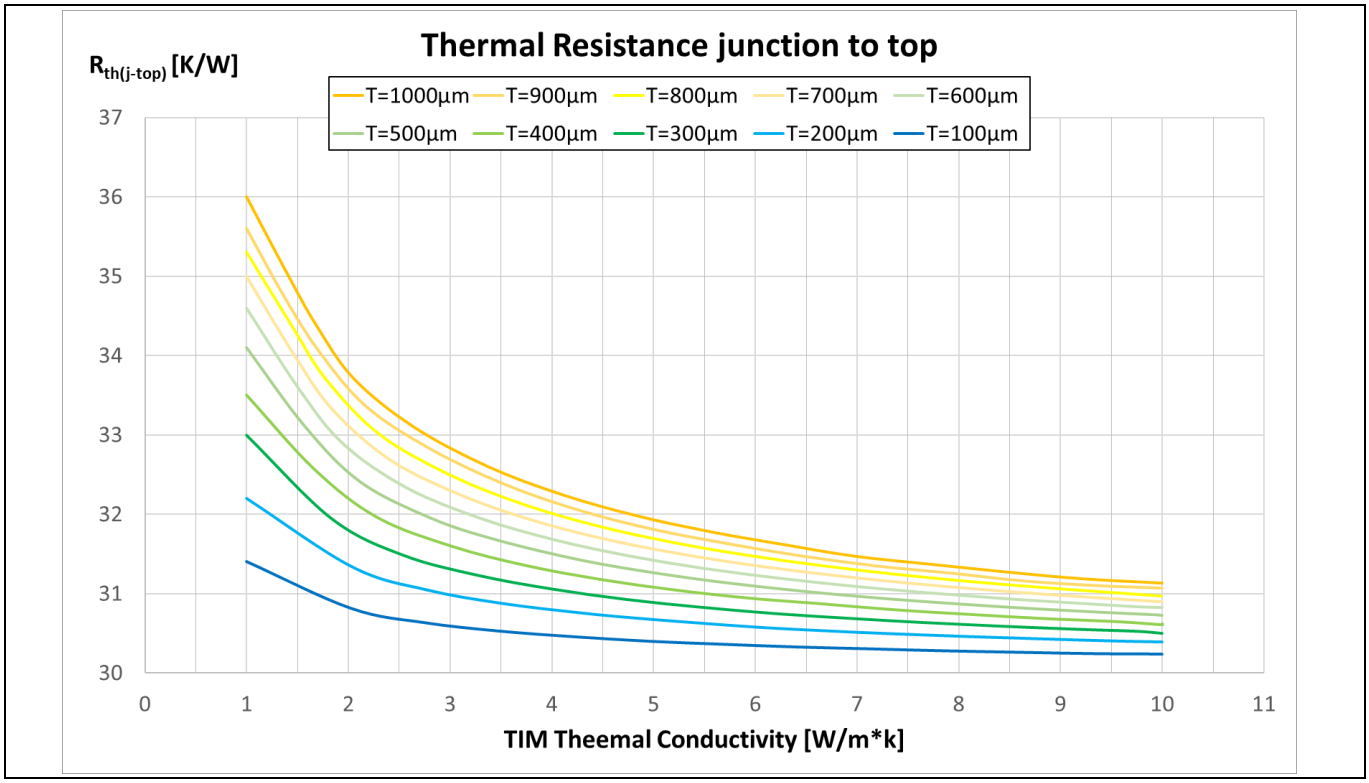


Figure 38 Effect of TIM conductivity and thickness on thermal resistance

Figure 38 shows the effect of the TIM thickness on the thermal performance of the product. As common sense might suggest, the thinner the TIM, the lower the thermal resistance, and the more conductive the TIM, again the lower the thermal resistance.

Looking at the scale, it is clear that in this particular case the impact is around 20 percent, from the ideal case of no TIM, where the thermal resistance is 30 K/W, to 36 K/W, when the TIM has the worst conductivity and forms a thicker layer.

Furthermore, it can be seen that beyond certain values of thickness and conductivity, the improvement becomes negligible, roughly 3 percent. Therefore, it is not always necessary to push the need for thermal conductivity and TIM thickness to extremes.

4.5 Heatsink connection

We saw in paragraph **3.2** that the component itself is quite robust against compression and bending, but the mounting of the heatsink should be done carefully due to second-level effects; therefore, during the mounting of the heatsink special precautions should be taken. [10] provides some basic indications for the HDSOP that can also be reused for 5x6 PQFN, as summarized here:

- The products considered in this application note are “low voltage”, so normally it is sufficient to follow the IPC-2221 rules for isolation distances. Furthermore, those products do not have leads coming out of the package, which might reduce the distance between the heatsink and the high-voltage nodes beyond the TIM. Nevertheless, it is suggested to use spacers to guarantee a minimum distance between the PCB and heatsink.
- The reason to guarantee a minimum distance is also related to the fact that the TIM has a maximum compression that should not be overcome. The risk is that in the long term the material loses mechanical properties and no longer performs as expected.

- Furthermore, depending on the size and shape of the heatsink, multiple connections between heatsink and PCB should be prepared in the layout phase to ensure than neither the PCB nor the heatsink will bend during the tightening of the screws.

5 Spice model

Electrical simulations might help to assess the benefits of the dual-side cooled compared with the bottom-side cooled. If a model of the actual converter with bottom-side cooled is already present, it will be easy to replace that model with an Infineon Spice model of the bottom-side cooled.

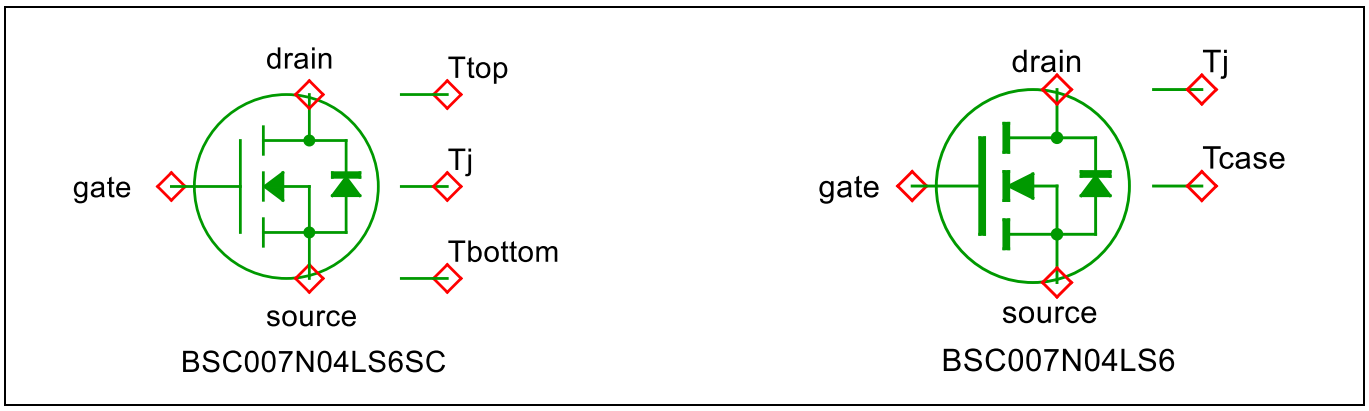


Figure 39 Infineon Technologies' simulation model for dual-side cooled (left) and bottom-side cooled (right)

Figure 39 shows the Infineon Technologies model for the dual-side cooled cooling. The main difference from a bottom-side cooled is the fact that now the device has six terminals, compared to five before. The new terminal (T_{top}) represents the top-side exposed pad with its own thermal impedance, given by the clip size and soldering structure.

To properly use the model, the customer needs to add a thermal network to the T_{top} terminal, which is representative of the structure composed of the TIM and heatsink.

6 Vertical current conduction

The use of vertical MOSFETs in the industry has already triggered the first experiments for vertical conduction [12].

The basic idea behind this concept is simple: common sense suggests that a good way to improve current conduction will also be good for heat conduction; for instance, increasing copper thickness in a layer will not only improve the resistance and conduction losses happening in that layer, but also will help to distribute the heat and therefore reduce the thermal resistance.

The exposed top pad of the Infineon Technologies dual-side cooled is solderable, since it is based on copper material; therefore, the top-side exposed pad could theoretically also be used not only for heat conduction but eventually also for current conduction. This would require soldering the top-side exposed pad to a copper bar, which will not only function as heatsink, but also as a current spreader.

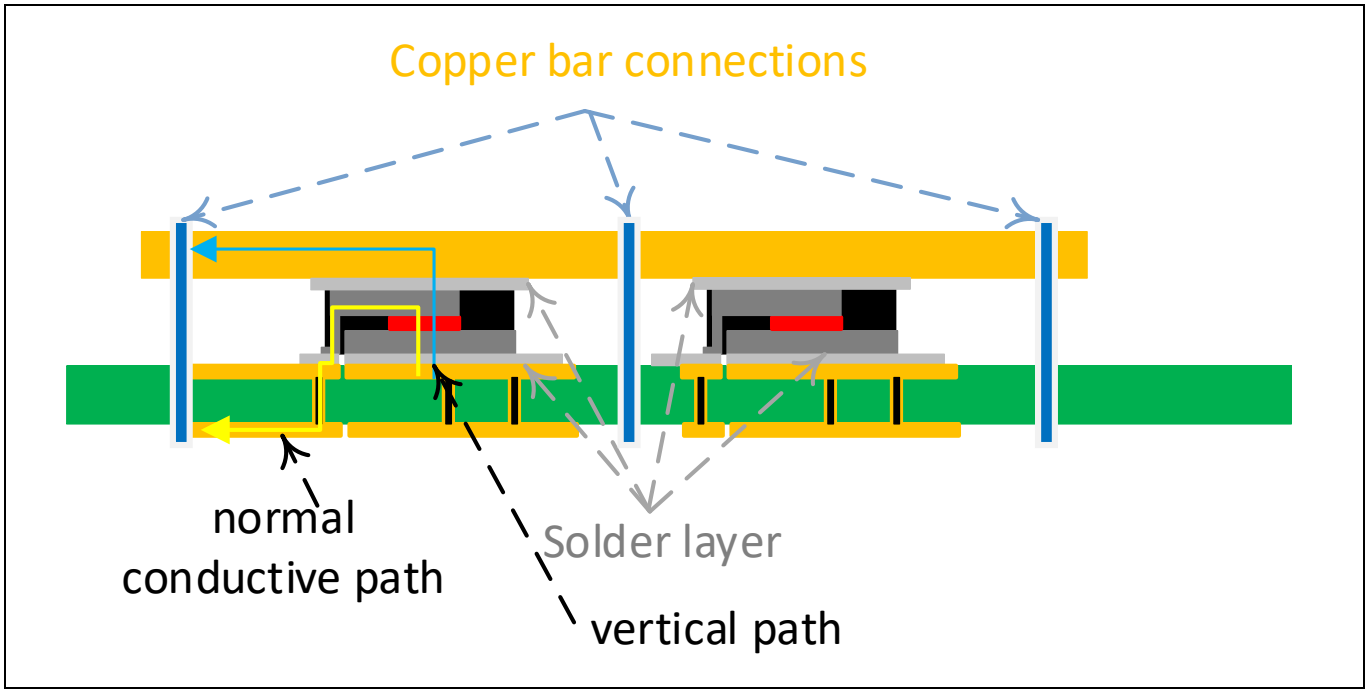


Figure 40 Vertical conduction (blue) vs. horizontal conduction (yellow)

Figure 40 shows the idea in principle. The current starting from the drain has the potential to flow through the horizontal paths of the clip and the PCB to come back to the initial point (the picture could represent a GND connection). It is evident that the same current, in case of a soldered heatsink on the top side of the dual-side cooled device, would go through the chip only vertically – without going through the horizontal path of the clip and proceeding on the horizontal path of the copper bar.

The benefits of the vertical conduction are as follows:

- There is no need to involve the horizontal part of the resistance of the clip in the current conduction path, therefore eliminating an important contribution to the overall electrical resistance.
- There is no need to go through the copper layers in the PCB, instead making use of the copper bar, which naturally has a much smaller electrical resistance compared to the layers in the PCB.
- The copper bar can also be used effectively as a heatsink.

However, the implementation of this simple idea is not that easy. There are the following challenges:

- First, the soldering of the copper bar has to be prepared in the entire process flow of the PCB mounting. It is possible that a second or a third reflow cycle must be implemented, introducing more risk to the process, compared to a simple mechanical attachment of the heatsink.
- Furthermore, a second stencil should be prepared to deposit the solder paste on top of the device in the right quantity. In fact, if too much solder paste is deposited a solder bridge might be formed between the top of the device and the bottom of the device (the device is only 0.5 mm high).
- The soldering of the bar would happen on top of the clip of the device; due to the different thermal coefficient expansions this could add some mechanical stress to the clip-die structure, which might compromise the device functionality immediately – or, even worse, decrease the lifetime due to the formation of micro cracks that won't be detected as an immediate failure in the functionality.

7 Summary

This paragraph collects the key points described in this document:

- **Table 10** provides very simple rules to help designers to choose when to use a dual-side cooled and bottom-side cooled; it is recommended in any case to design the layout to host both footprints.
- **Table 11** delivers a short list of dual-side cooled benefits.
- **Table 12** offers a list of simple recommendations for dual-side cooled best practice.

Table 10 dual-side cooled and bottom-side cooled use cases

Condition	dual-side cooled	bottom-side cooled
Board size	Board the size of the power MOSFETs' area	Board bigger than the power MOSFETs' area
Board copper content	Board has a very low copper content (one or two layers of only 1 oz.)	Board has many layers of thick copper (more than two layers of 2 oz)
Load behavior	Load has high excursions; peak load can be two to three times or more than the typical load; effectively a low thermal capacitance is more of a requirement than low thermal resistance	Load has low excursions; peak load is just few percentage points above the typical load; low thermal resistance is required and the thermal capacitance provided by the PCB is sufficient
Other heat sources	The board contains multiple sources of heat that are somehow connected by the same copper trace and concentrated in a small area of the PCB	The multiple sources are split around the PCB and do not share power traces

Table 11 dual-side cooled benefits

Device property	Customer benefit
Lower thermal resistance from junction to top compared to bottom-side cooled	Possibility to add a heatsink, with the following benefits: • Increase peak and steady-state power density (20 to 40 percent) • Reduce PCB temperature (higher reliability) (20 percent) • Equalize temperatures among similar devices
Footprint and part number compatibility with SuperSO8	Easy drop-in replacement for increased power density with minimum evaluation effort

Summary

Table 12 dual-side cooled best practice

Process	Recommendations
Soldering to the board	Tombstone effect: pay attention to the layout and soldering process, to avoid vertical tilting of the device, with risk of hot spots
Vias under pad	Capillary effect: quantity, diameter hole and pitch should be adjusted to the solder process
TIM	Minimize thickness, but not beyond the suggested value. Consider the mechanical stress applied during the heatsink mounting and thermo-mechanical stress during lifetime.
Heatsink mounting	Minimize mechanical stress of components placed under the heatsink and possibility of bending of PCB or heatsink (three-point heatsink connection)

8 References

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