Paralleling MOSFETs in high-current LV drive applications

About this document

Scope and purpose

MOSFETs are in most cases easy to control with the right driver.

When switched in parallel, control becomes more tricky. Despite the fact that the $R_{DS(on)}$ has a positive temperature coefficient, paralleling of MOSFETs is not a simple topic; an unbalanced circuit with increased losses or even destruction could be the result if it is not done properly. The influences on the balancing of current are shown in this application note.

Intended audience

Designers of high-current applications.

Table of contents

About this document . . . 1

1 Introduction . . . 2

2 Switching behavior of a MOSFET . . . 3

2.1 Theoretical gate-to-source voltage . . . 3

2.2 Real gate-to-source voltage . . . 4

2.3 Simplified gate-to-source voltage with parasitics . . . 4

2.3.1 Turn-on process . . . 4

2.3.2 Turn-off process . . . 5

3 Circuit definition for simulation and PCB . . . 7

3.1 PCB for measurements . . . 7

3.2 Simulation circuit . . . 8

4 Analysis . . . 9

4.1 Influence of the MOSFETs' bond wire source inductance . . . 9

4.2 Influence of tolerances of the external gate resistor $R_{G,ext}$ . . . 11

4.3 Influences of the gate threshold voltage V_{GSth} . . . 13

4.4 Asymmetrical/unbalanced layout . . . 17

5 Summary . . . 21

6 Revision history . . . 22

Disclaimer . . . 23

1 Introduction

Articles and application notes about the “perfect” layout are common. The standard rules, such as avoiding loops and choosing the right copper diameter for tracks and wires, are well known and are not part of this application note.

MOSFETs are powerful electronic switches, and in most cases they are more or less easy to control.

But like all electronic switches they are not ideal. Especially in applications with a higher power rating, the job can become trickier.

Above a certain power level one MOSFET per switch is not sufficient. Paralleling MOSFETs seems to be very easy at first, but in reality it can be more difficult. This is due to the tolerances of the devices themselves and the parts around them. Additionally the layout can unbalance the circuit, leading to a non-ideal behavior.

Chapter 1 explains why the measured waveforms don’t reflect the real behavior of the MOSFET.

Chapter 3 explains the set-up for the measurements and the simulation.The comparison of different reasons for an unbalanced set-up starts from ***Chapter 4*** onwards.

It shows the differences in switching waveforms and losses, showing both simulated and measured diagrams and figures.

Due to package parasitics caused by bond wires etc. the measured waveforms do not show completely what happens on the chip level.

2 Switching behavior of a MOSFET

To understand the analyzed waveforms of the simulations and the measurements it is necessary to understand how a MOSFET turns on and off. The following diagram describes the $V_{GS,int}$ (internal gate source voltage), V_{DS} (drain source voltage), I_D (drain current) and the voltage over the internal source inductivity $V_{L,SOURCE}$ in a simplified visualization of the turn-on and turn-off phase.

2.1 Theoretical gate-to-source voltage

$V_{GS,int}$ is the “real” gate-to-source voltage on the chip level, while V_{GS} the externally measured one.

The dotted line represents the complete MOSFET in a package.

Without parasitic inductances and the internal gate resistor $R_{G,int}$ the internal and external gate-to-source voltages would be identical, as in this figure:

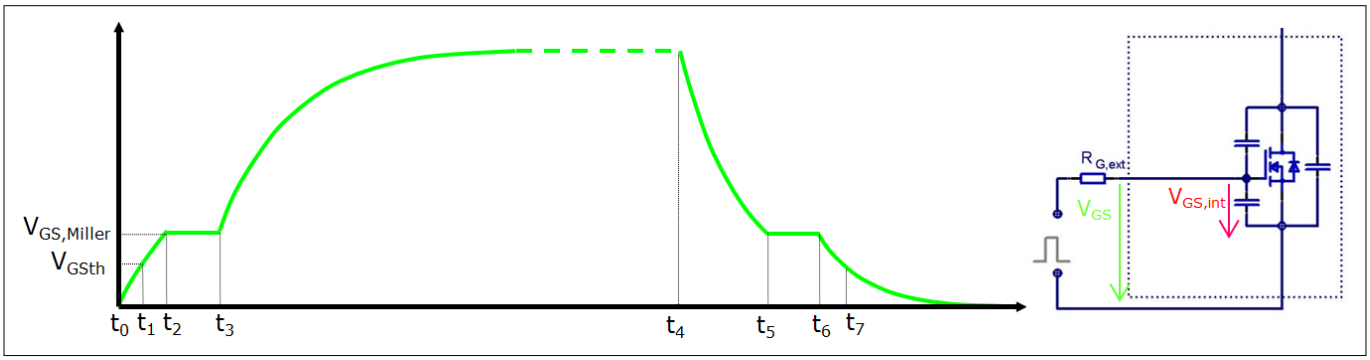

Figure 1 V_{GS}: Theoretical turn-on and turn-off process of a MOSFET

t_0: The driver’s output transfers from “low” to “high” and V_{GS} starts to increase

t_1: V_{GS} reaches the threshold voltage V_{GSth} and the drain current I_D starts to flow

t_2: The drain current I_D reaches (nearly) the maximum value and the Miller plateau starts

t_3: The Miller plateau is crossed and V_{GS} continues to increase to its maximum

t_4: The driver’s output transfers to “low” and V_{GS} starts to decrease

t_5: Miller plateau starts

t_6: I_D starts to decrease

t_7: V_{GS} reaches the V_{GSth}, current drops to zero

2.2 Real gate-to-source voltage

In reality the waveforms look as shown in ***Figure 2***, which is completely different to the theoretically expected waveforms.

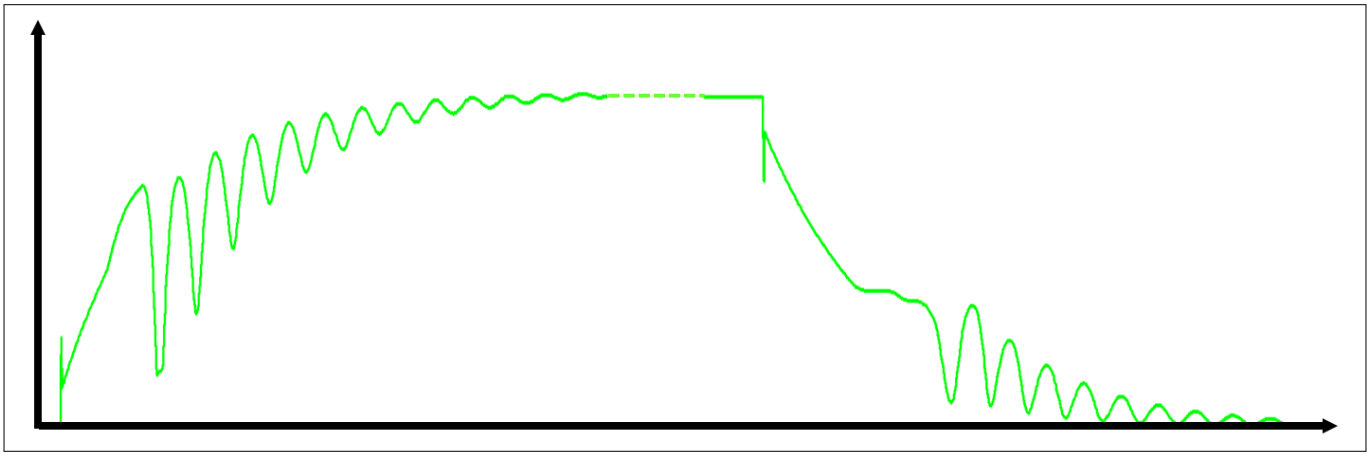

Figure 2 V_{GS}: Real turn-on and turn-off process of a MOSFET

The waveform looks even more different when MOSFETs are used in parallel, as in ***Figure 3***.

In theory both waveforms should be exactly the same. In reality they are completely different during the switching processes.

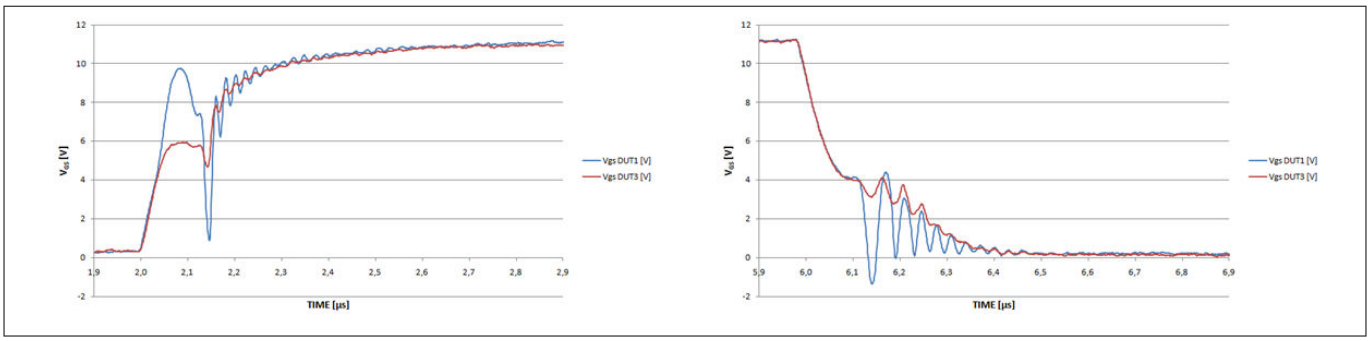

Figure 3 V_{GS}: Real turn-on and turn-off process of a MOSFET in a non-balanced circuit

2.3 Simplified gate-to-source voltage with parasitics

To understand the differences between theory and reality it is necessary to have a closer look at the separate phases of the turn-on and turn-off process. To aid understanding the waveforms are simplified.

2.3.1 Turn-on process

The turn-on process can be separated into four phases.

2 Switching behavior of a MOSFET

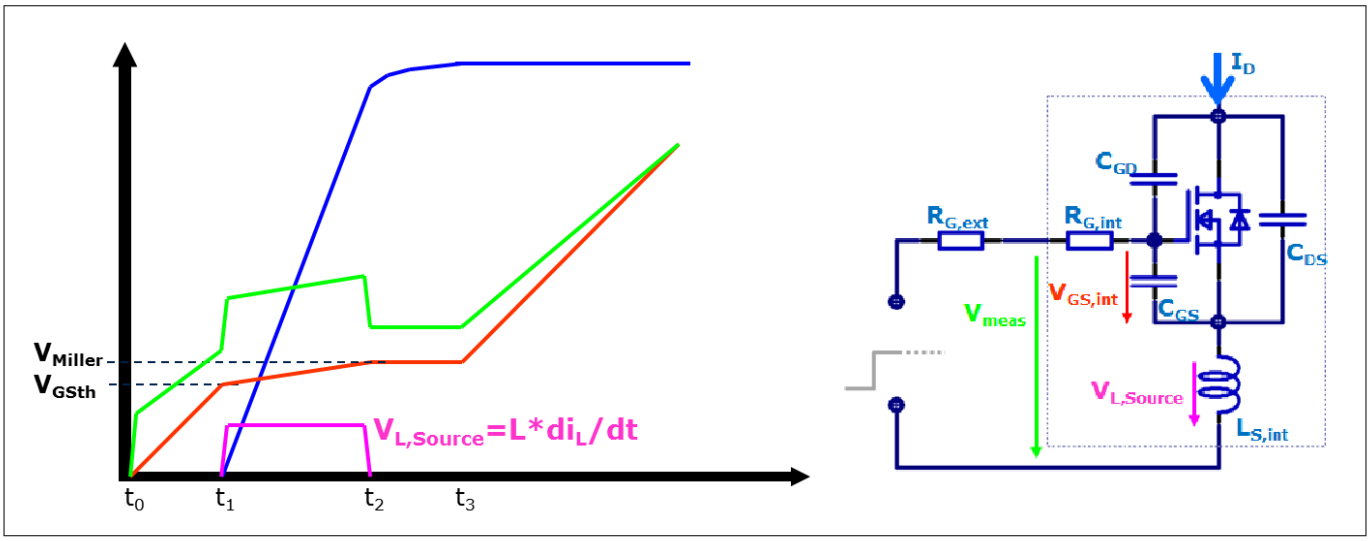

Figure 4 Turn-on process of a MOSFET

t_0: The driver's output transfers to "high" and $V_{GS,int}$ (red) starts to increase slowly. Externally a steep step in the $V_{GS,ext}$ (green) is visible. The reason is the voltage divider $R_{G,ext}$ vs $R_{G,int}$.

t_1: $V_{GS,int}$ reaches the threshold voltage V_{GSth} and the drain current I_D (blue) starts to flow with a certain di/dt. The voltage due to the parasitic source inductance (purple) is added on top of the $V_{GS,ext}$, resulting in an additional step.

t_2: The drain current I_D reaches (nearly) the maximum value and the Miller plateau starts. The di/dt drops to zero, e.g. $V_{L,Source}$ = 0 V, resulting in a decrease of the $V_{GS,ext}$. It looks like the MOSFET is turned off again even if the $V_{S,int}$ on the chip level isn't increased.

t_3: The Miller plateau is crossed and V_{GS} continues to increase to its maximum. The MOSFET is now switched on completely, and a further increased V_{GS} results only in a further reduction of the $R_{DS(on)}$.

2.3.2 Turn-off process

The turn-off process can also be separated into three phases.

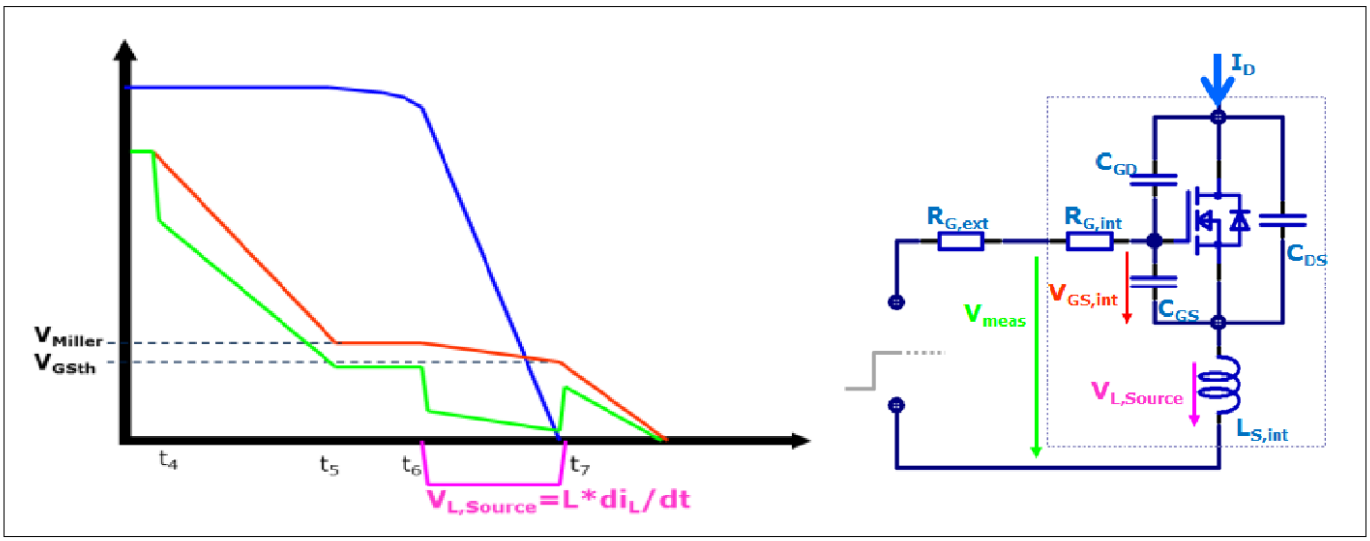

Figure 5 Turn-off process of a MOSFET

t_4: The driver's output transfers to "low" and $V_{GS,int}$ (red) starts to decrease slowly. Externally a steep step in the $V_{GS,ext}$ (green) is visible. The reason is again the voltage divider $R_{G,ext}$ vs $R_{G,int}$.

2 Switching behavior of a MOSFET

t_5: $V_{GS,int}$ reaches the Miller plateau and the MOSFET starts to switch off. The V_{DS} (not shown) goes from ~ 0 V to the blocking voltage.

t_6: The drain current I_D (blue) starts to decrease with a certain di/dt. The voltage due to the parasitic source inductance (purple) is now subtracted from the $V_{GS,ext}$, resulting in a step down.

t_7 The $V_{GS,int}$ reaches the threshold voltage V_{GSth} and the drain current I_D drops to zero. The di/dt is now also zero, e.g. $V_{L,Source}$ = 0 V, resulting in a positive step of the $V_{GS,ext}$. It looks like the MOSFET is turned on again even if the $V_{S,int}$ on the chip level isn't increased. The MOSFET is switched off completely.

3 Circuit definition for simulation and PCB

This chapter is going to describe the realized circuit for the simulation. For the first step it is necessary to define the fundamental set-up of the simulation circuit. After this, it is obligatory to realize this circuit on a PCB and in the next step the circuit of the simulation has to be approximated to the real PCB. This step is essential because the PCB has parasitic inductances due to the length of the copper tracks. For a comparison between simulation and real behavior these inductances have to be implemented in the simulation circuit.

3.1 PCB for measurements

All measurements were done using this PCB:

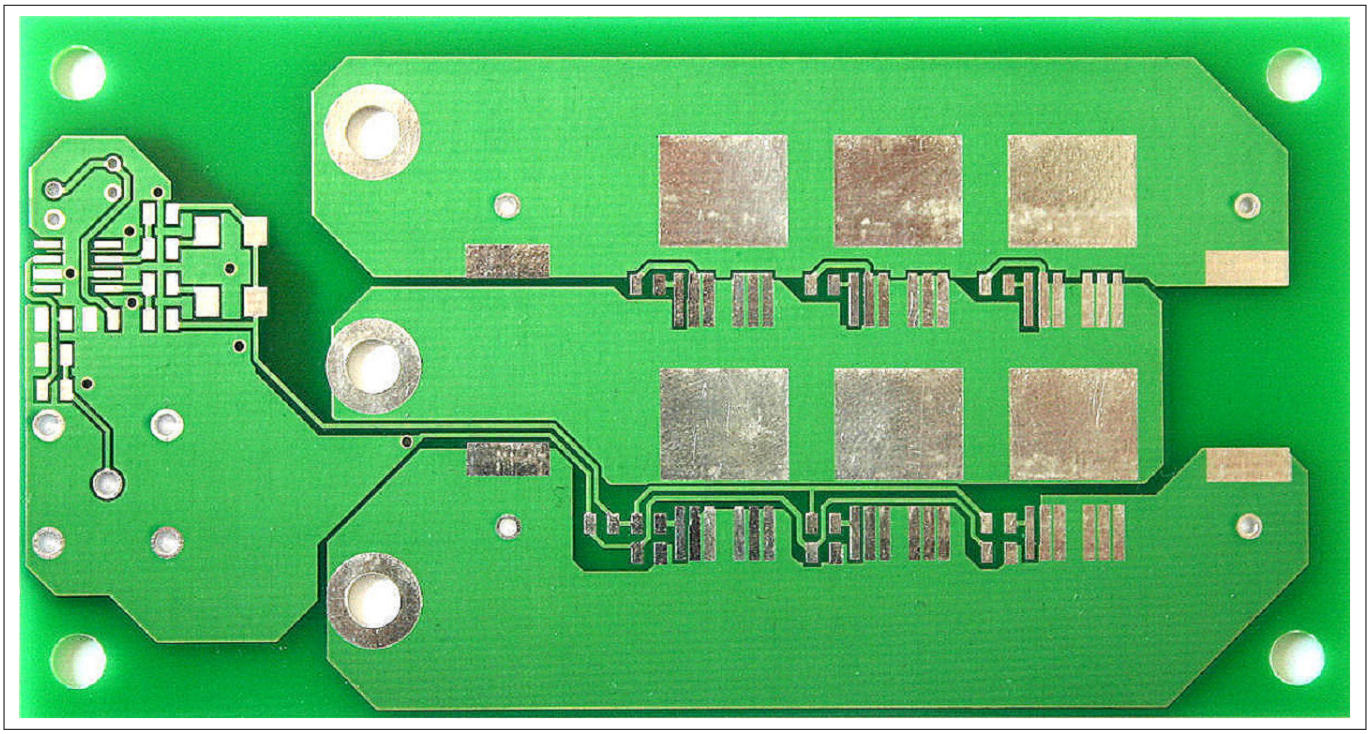

Figure 6 PCB for measurements

Originally this was designed as a complete half-bridge to allow the paralleling of up to three MOSFETs per switch.

It's a single-layer PCB similar to the standard Insulated Metal Substrate (IMS) used in high-power drive applications like forklifts and Light Electric Vehicles (LEVs).

For the measurements only two MOSFETs (DUT1 and DUT3) were assembled as active switches on the low-side, and only one on the high-side acting as a freewheeling diode.

3.2 Simulation circuit

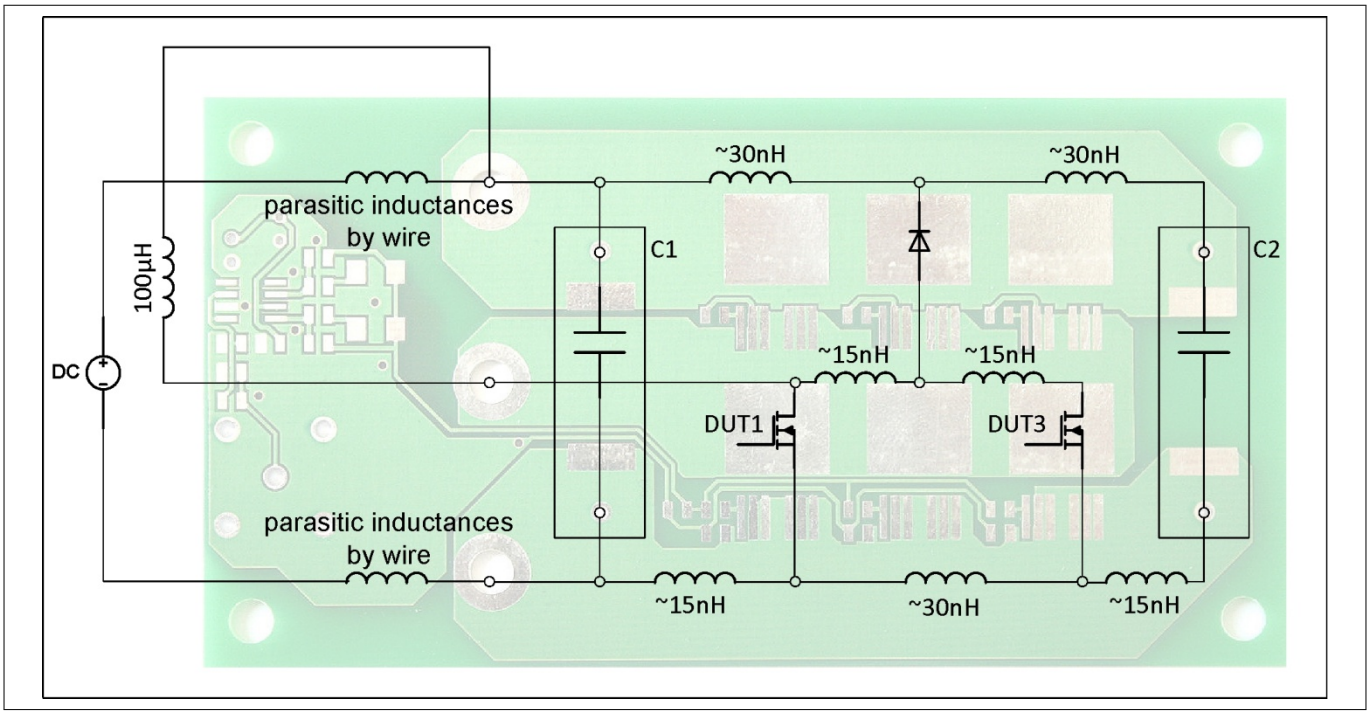

Figure 7 Modified simulation circuit

For the simulation the simplified schematic in ***Figure 7*** was used.

The figures of the parasitic inductances were estimated using the rule of thumb:

1 cm track length can be assumed to be around 10 nH. Of course this figure depends on the layout, but for a start these figures are sufficient.

4 Analysis

All the comparisons between simulation, measurement and the corresponding influences of the components mentioned will be analyzed. Before starting with the analysis, it is important to know that it is not possible to measure the current on the PCB (through the paralleled MOSFETs) accurately. It would be necessary to add a shunt resistor to the circuit and measure the voltage over it, but this resistor could influence the switching behavior and the measurements would not be correct. Therefore, it is obligatory to compare the waveforms of the V_{GS} and V_{DS} of the measurements and the simulations.

All the differences in the switching behavior when implementing different $R_{G,ext}$ source inductances or MOSFETs with different V_{GSth} are compared to a completely symmetrical set-up, which is marked as a reference set-up (Ref).

Simulations and measurements are performed at 10 kHz, a typical switching frequency in high power drive applications.

For each set-up, both simulated and measured V_{GS} (DUT1 and DUT3) waveforms are shown.

4.1 Influence of the MOSFETs' bond wire source inductance

The assembly of the bond wires and the placement of the MOSFETs on the PCB causes small differences in the source inductance of each device.

To see the influences of the source inductivity, it is assumed that a 2 nH inductance is added to the source of the DUT3. The sum of the internal and external source inductance now has the value of 4 nH, twice the value of DUT1.

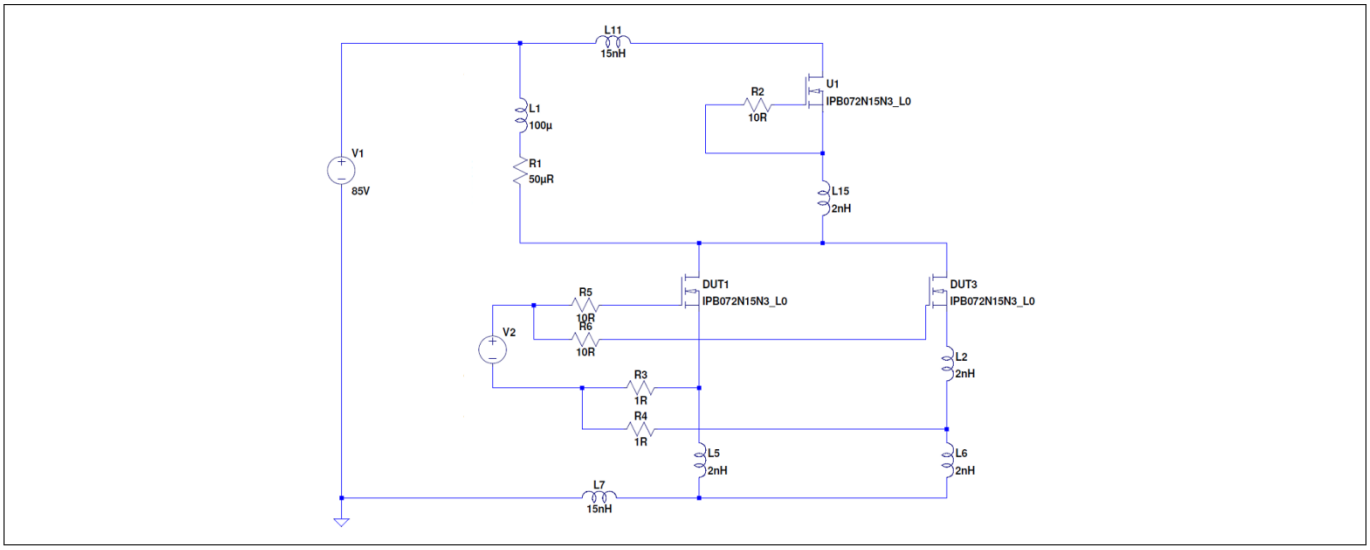

Figure 8 Simulation schematic: Increased source inductance in one leg

4 Analysis

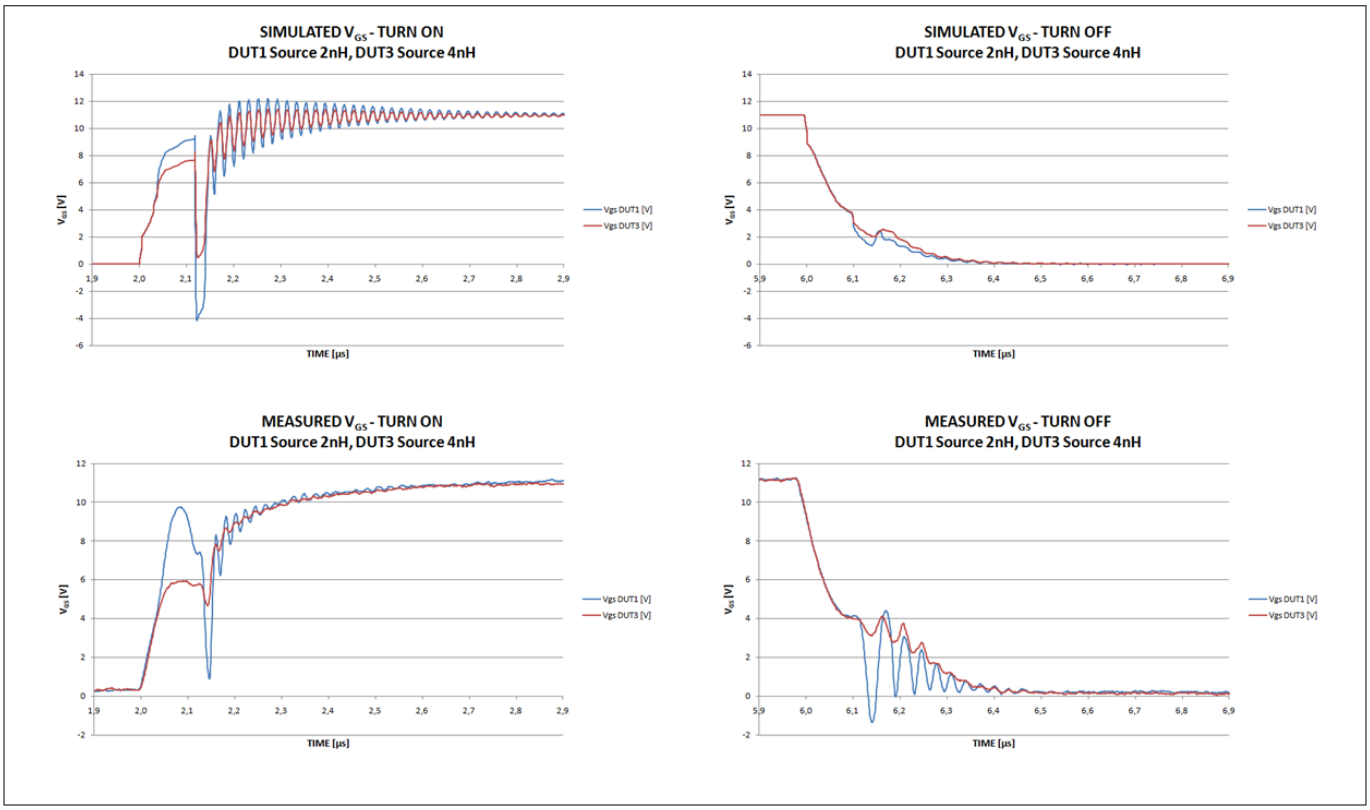

Figure 9 Comparison simulation vs measurement, 2 nH additional source inductance at DUT3

The reason for the V_{GS} differences between DUT1 and DUT3 were explained in section ***Chapter 2.3***.

During turn-on the higher di/dt in DUT1 (blue) caused by the lower source inductance results in the much higher V_{GS}.

During turn-off, again the lower source inductance causes a higher di/dt, but this figure is negative, reducing the V_{GS} of DUT1 during the switching process.

4 Analysis

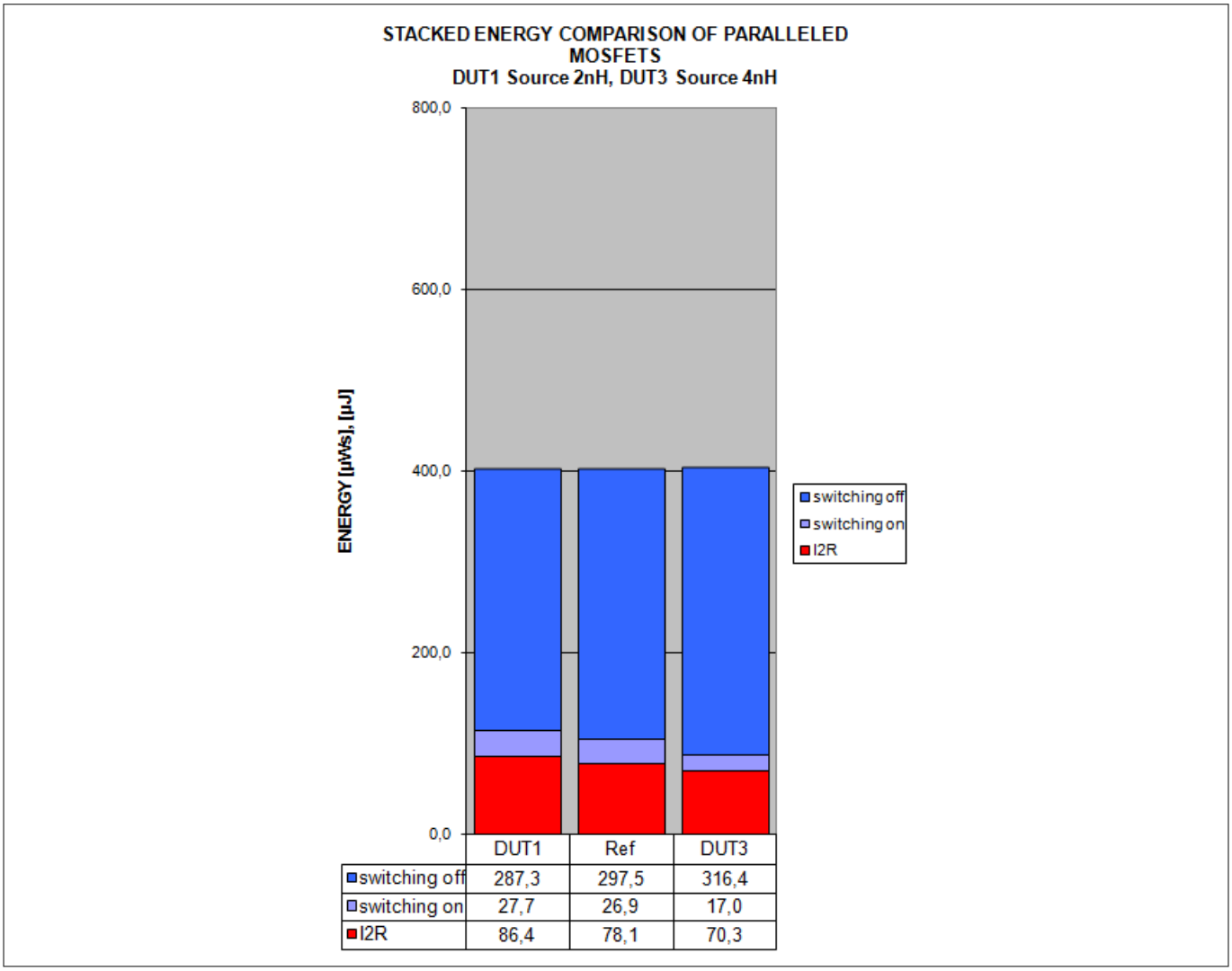

Figure 10 Losses in different phases

Figure 10 illustrates the losses in the different time frames. To be independent of the switching frequency the losses are shown here in µJ "per shot," e.g. one single 100 µs pulse.The overall losses are almost the same for DUT1, DUT2 and "Ref" (the reference MOSFET in an absolutely balanced circuit). "I2R" losses are the $R_{DS(on)}$ losses.

In the figures above, it is shown that there is a qualitative equal waveform in comparison of the simulation and the measured values.

Furthermore, it is clear that the VGS from DUT1 and DUT3 starts to behave differently when the current begins to flow. Then there is a higher voltage drop over the source inductance of DUT3. After the maximum current is reached there is no change of the current slope, and the VGS of DUT1 and DUT3 are equal again. This behavior is shown in the turn-on and turn-off phases of the MOSFETs and is completely different in comparison to the influences of the external gate resistor. This is covered in the next chapter.

4.2 Influence of tolerances of the external gate resistor $R_{G,ext}$

Like every electronic part the external gate resistor shows tolerances. A higher resistance leads to a later switching. Assuming a tolerance of +/-10 percent results in this schematic:

4 Analysis

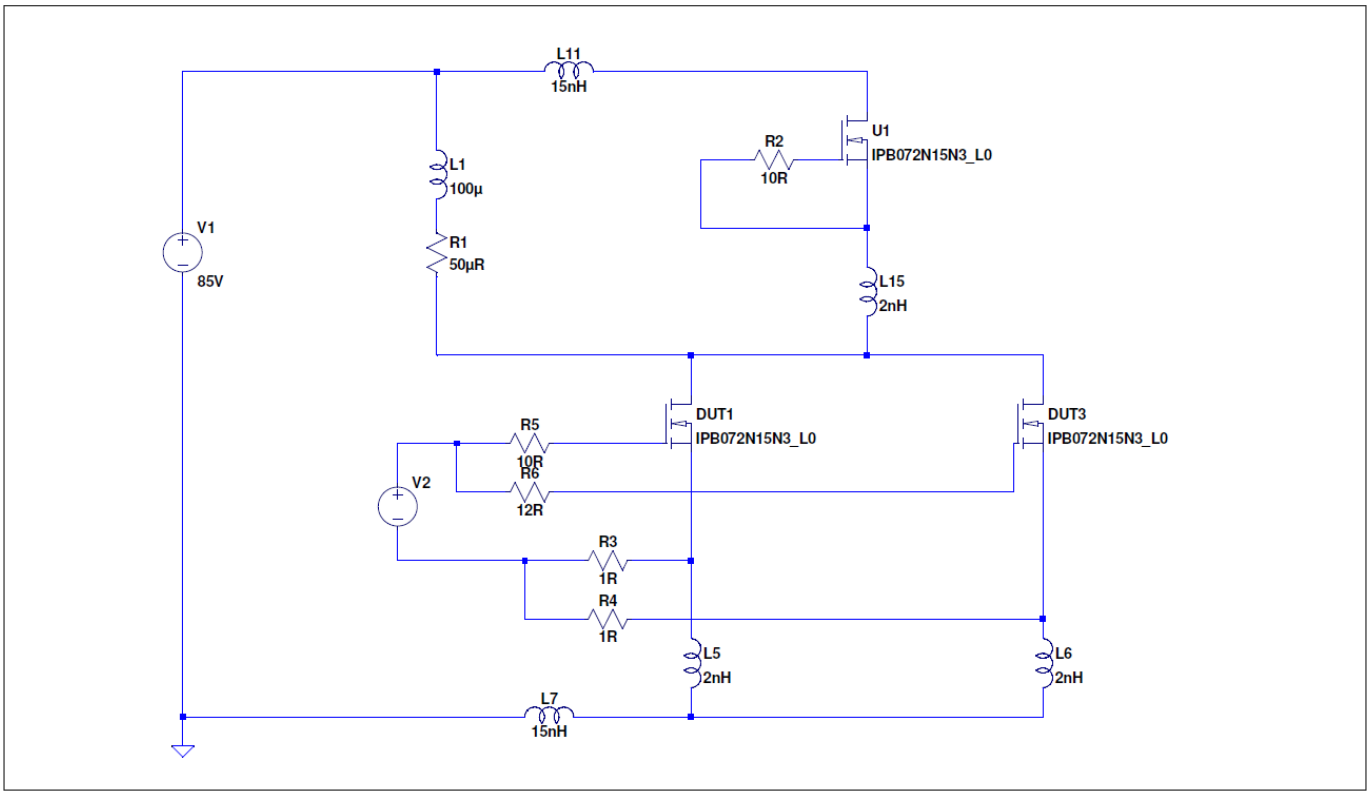

Figure 11 Set-up with different external gate resistors

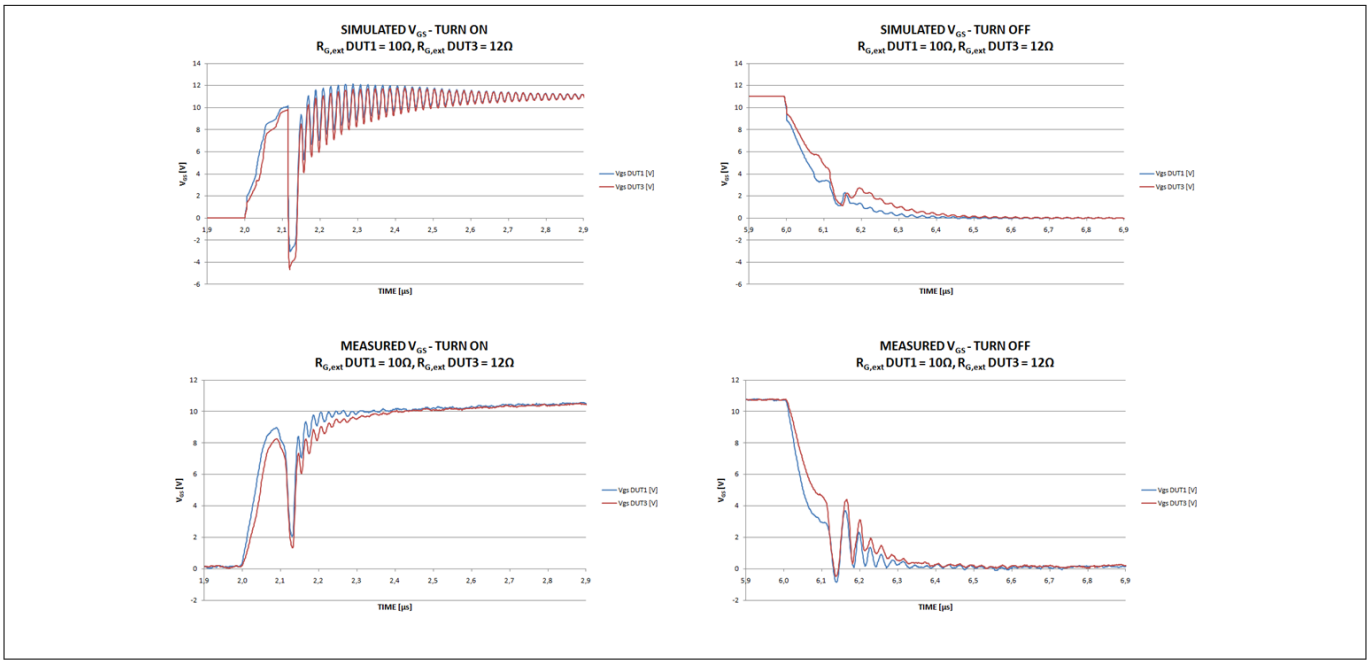

Figure 12 Comparison simulation vs measurement ($R_{G,ext}$)

4 Analysis

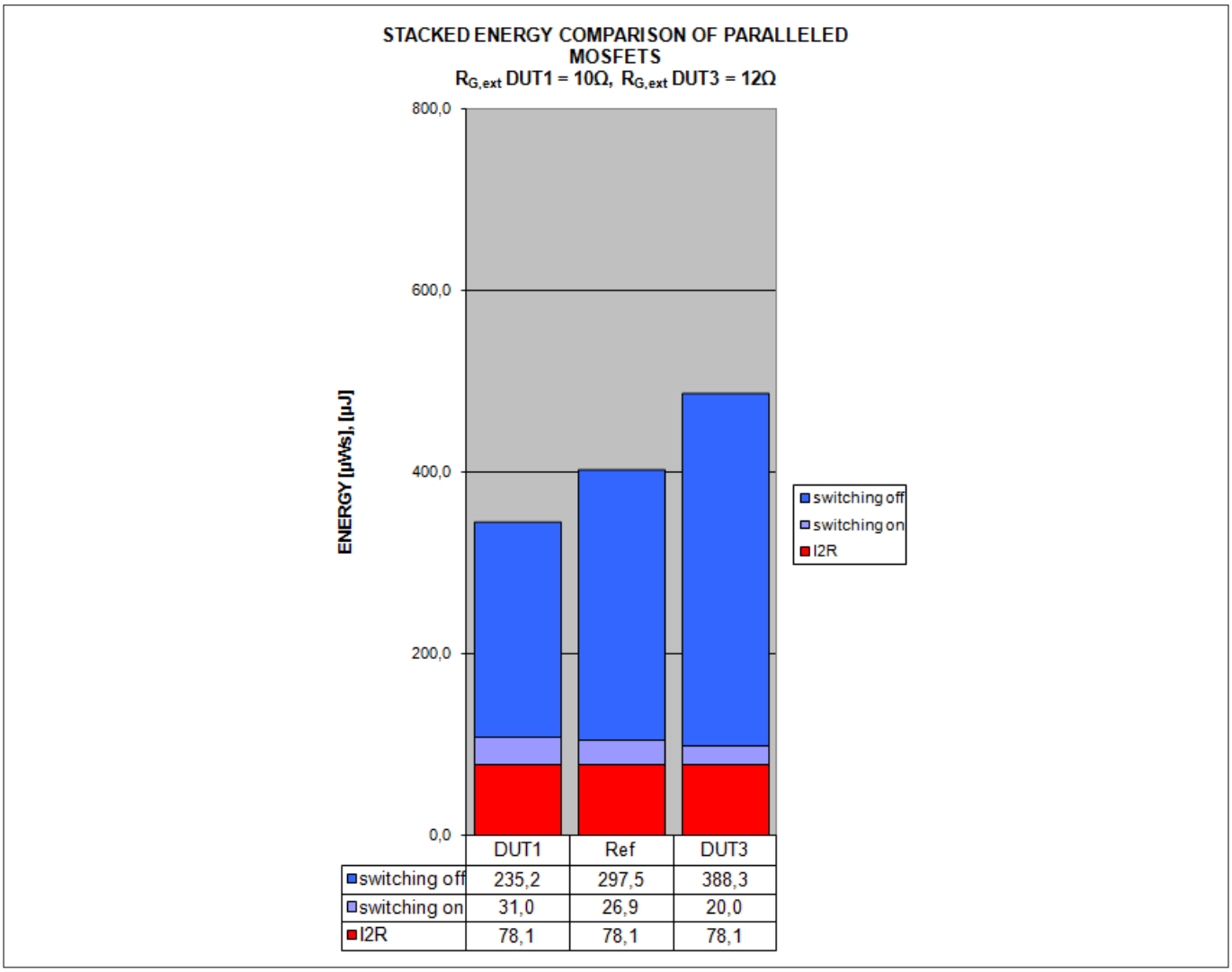

Figure 13 Losses with two different external gate resistors

During the switching-off process the MOSFET with the higher gate resistance shows the higher losses.

There are almost no influences on the switching behavior, because when using an RG,ext of, for example, 10 Ω with a tolerance of ±5 percent or less for DUT1 and DUT3 the worst-case scenario would be DUT1 with 9.5 Ω and DUT3 with 10.5 Ω. With this constellation there would be an energy dissipation, which is displayed in ***Figure 13***.

4.3 Influences of the gate threshold voltage V_{GSth}

The VG_{Sth} of a MOSFET of the IPB072N15N can vary from 2 V to 4 V at room temperature.

Assuming the worst case variation leads to this schematic:

4 Analysis

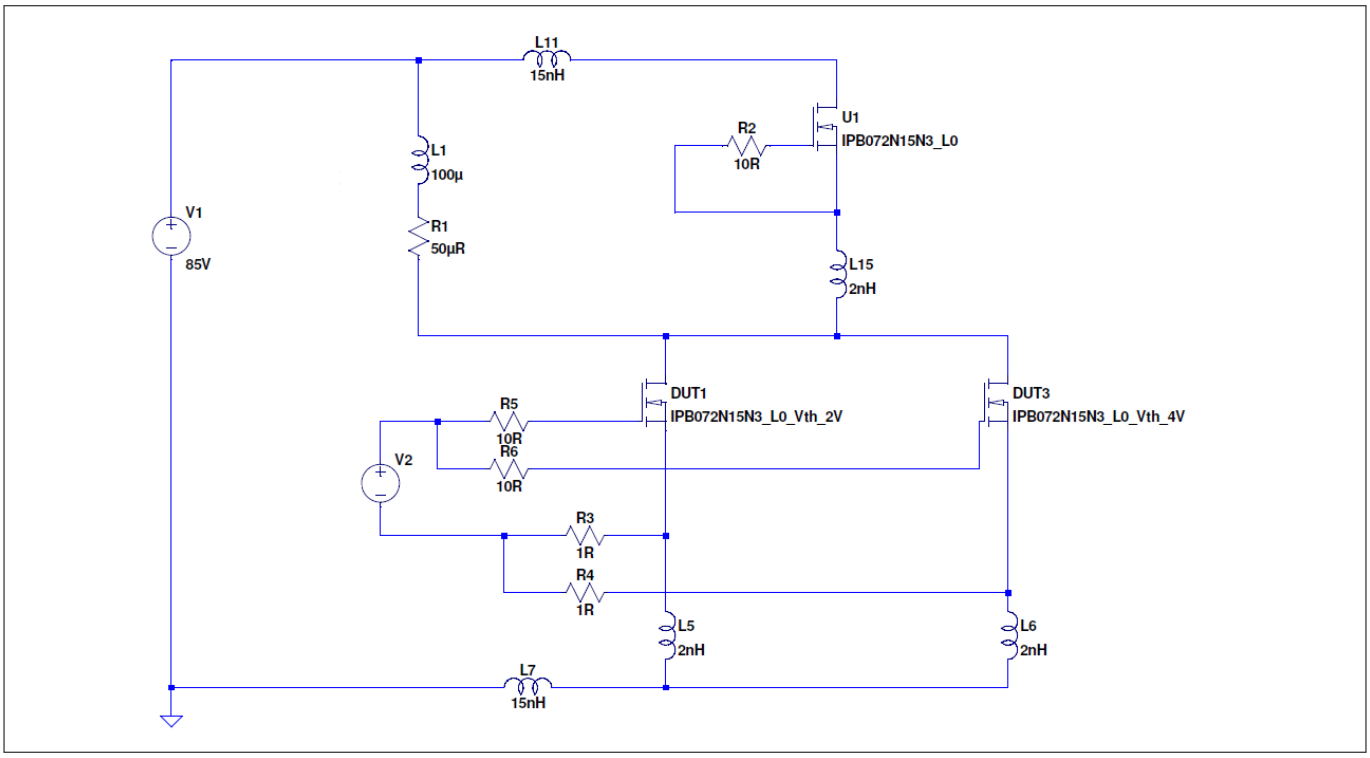

Figure 14 Simulation schematic for V_{GSth} variations

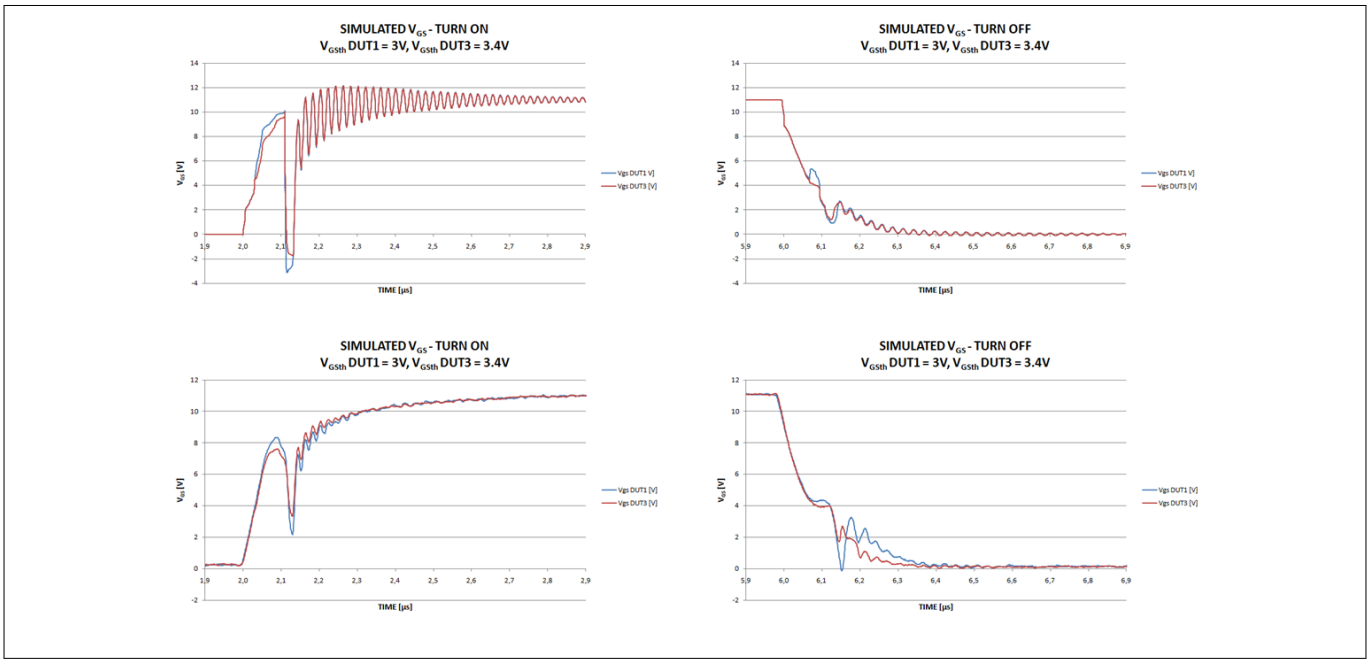

Figure 15 V_{GSth}: Comparison simulation vs measurement

4 Analysis

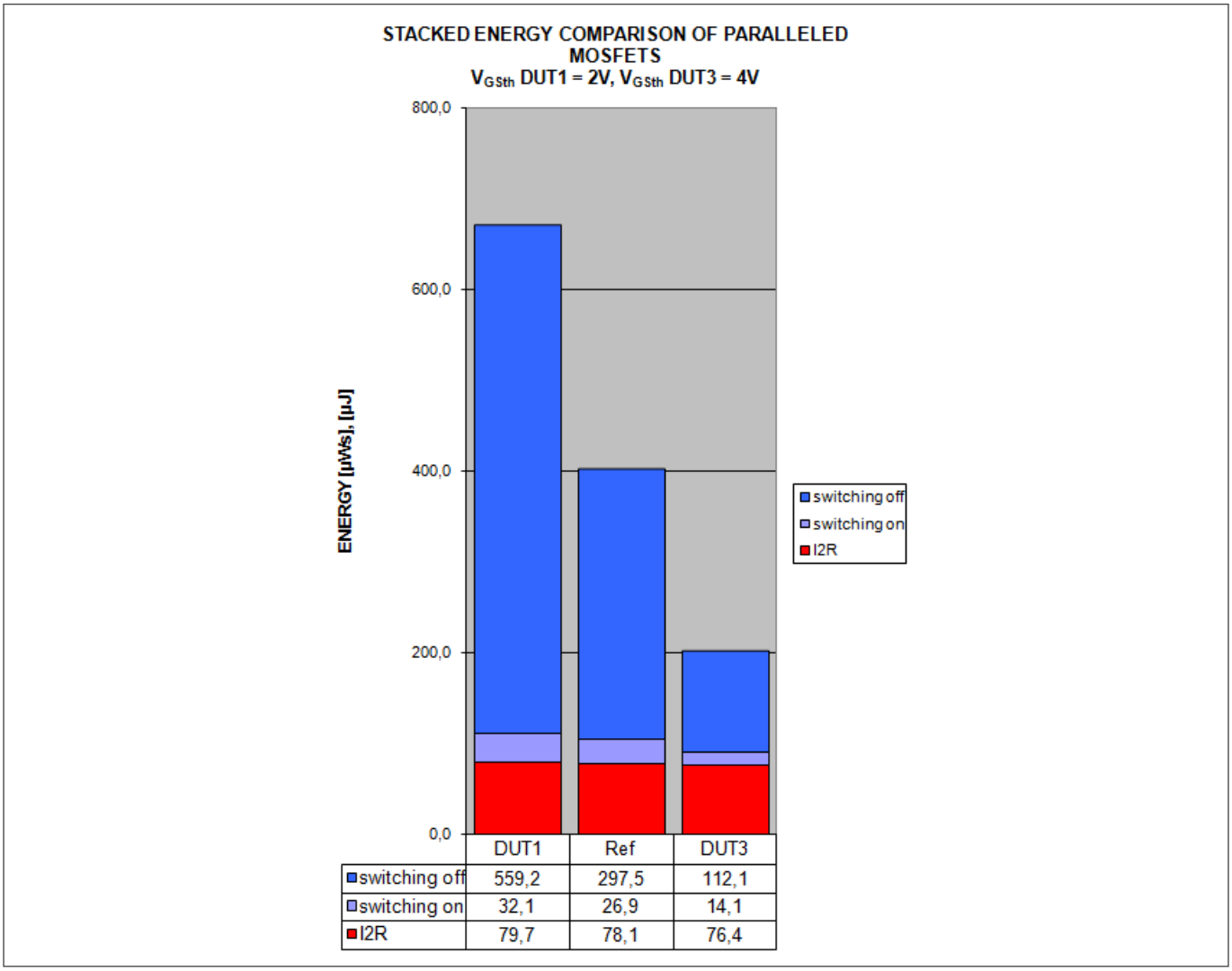

Figure 16 Losses with worst-case V_{GSth} variation (2 V to 4 V)

Again, the losses during switching off are much higher than during switching on.

If non-merged lots are used the differences in one lot are much lower. Assuming a difference of only 0.4 V reduces the differences significantly.

4 Analysis

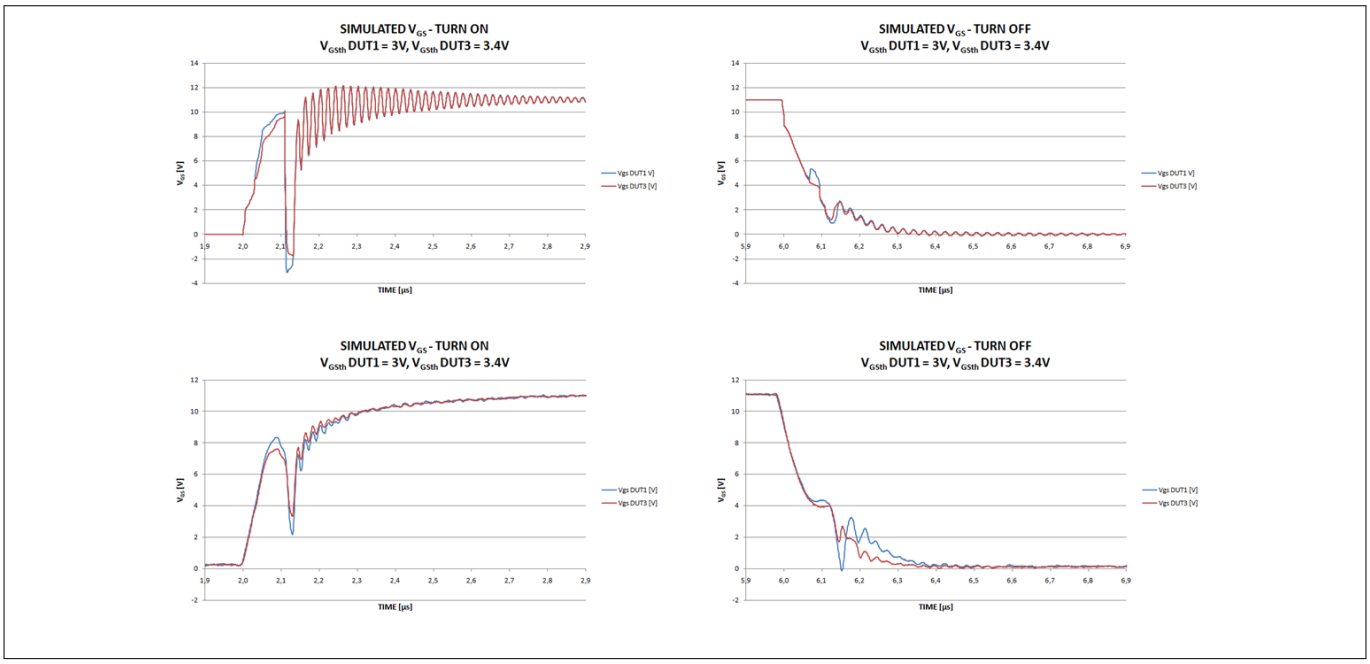

Figure 17 V_{GSth}: Comparison of simulation vs measurement

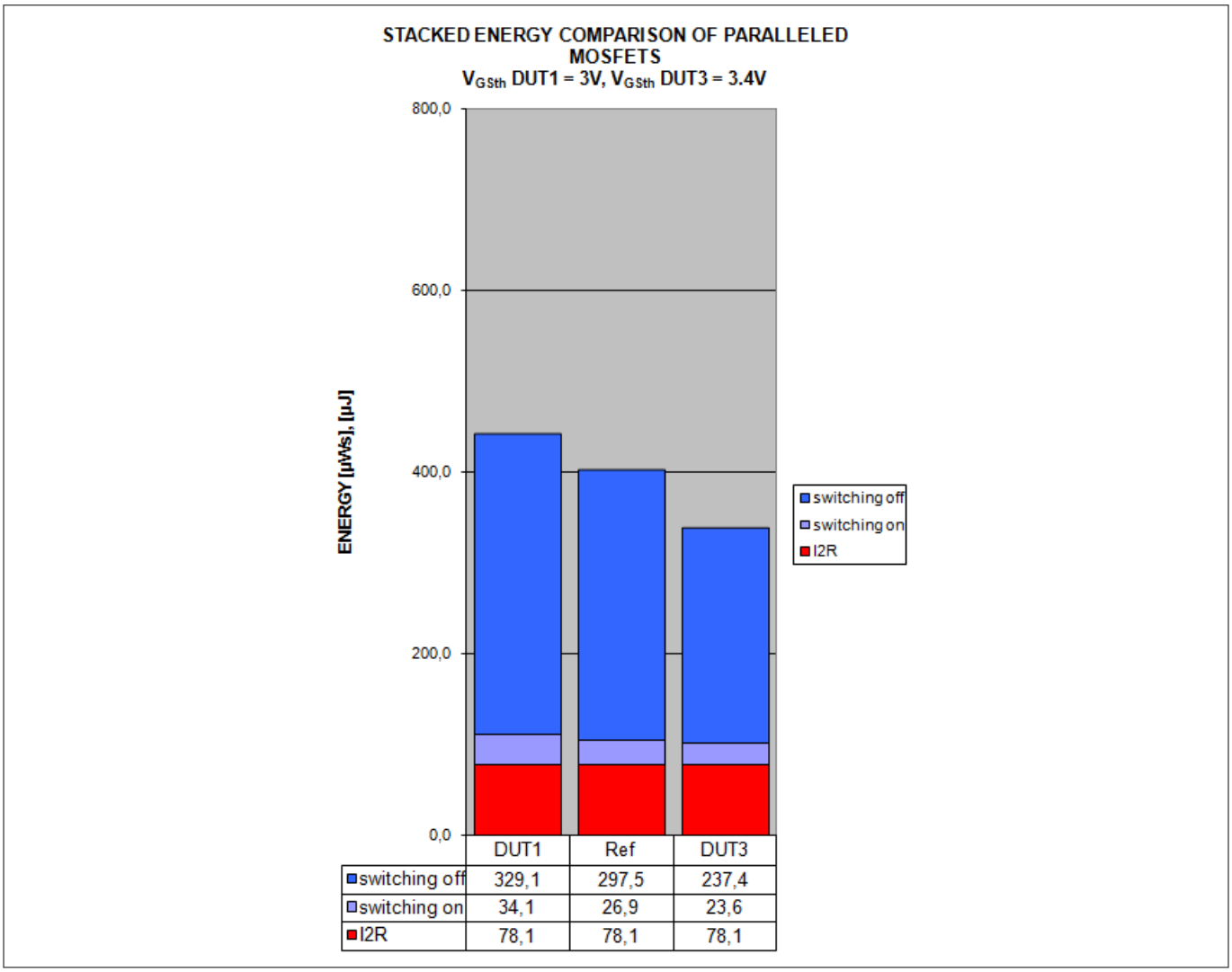

Figure 18 Losses with 0.4 V_{GSth} variation

4.4 Asymmetrical/unbalanced layout

If a circuit is not perfectly balanced the switching behavior can vary significantly.

Assuming ~ 10 nH for 1 cm of copper track leads to this circuit:

4 Analysis

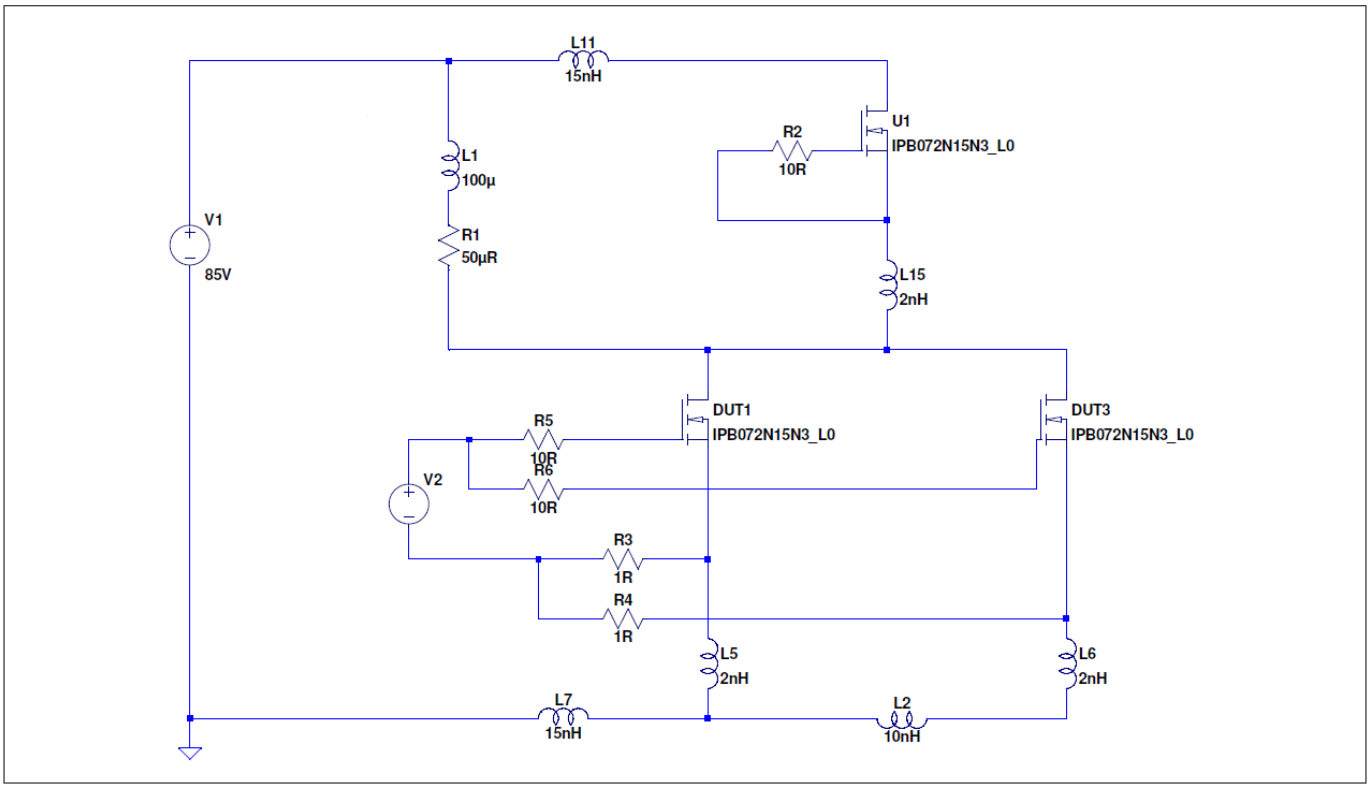

Figure 19 Simulation schematic for an asymmetrical layout

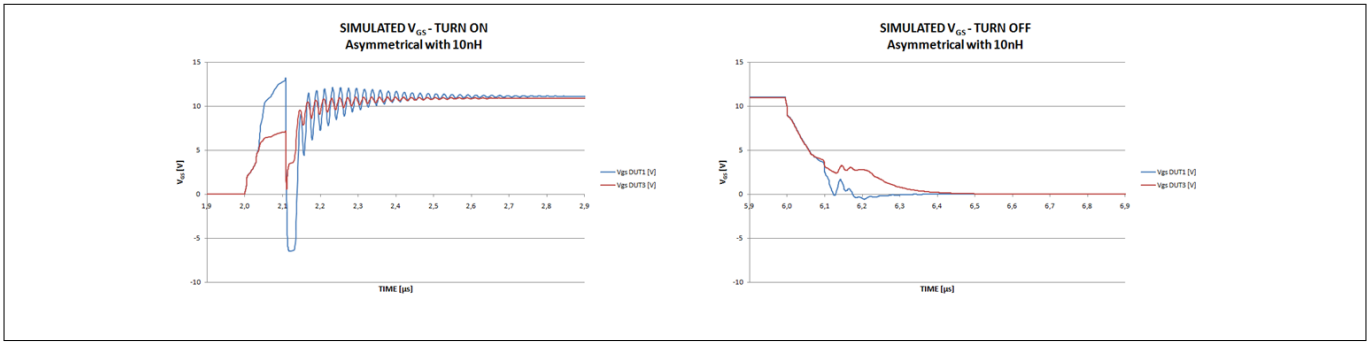

Figure 20 V_{GS} of DUT1 and DUT3 of an asymmetrical layout (10 nH)

4 Analysis

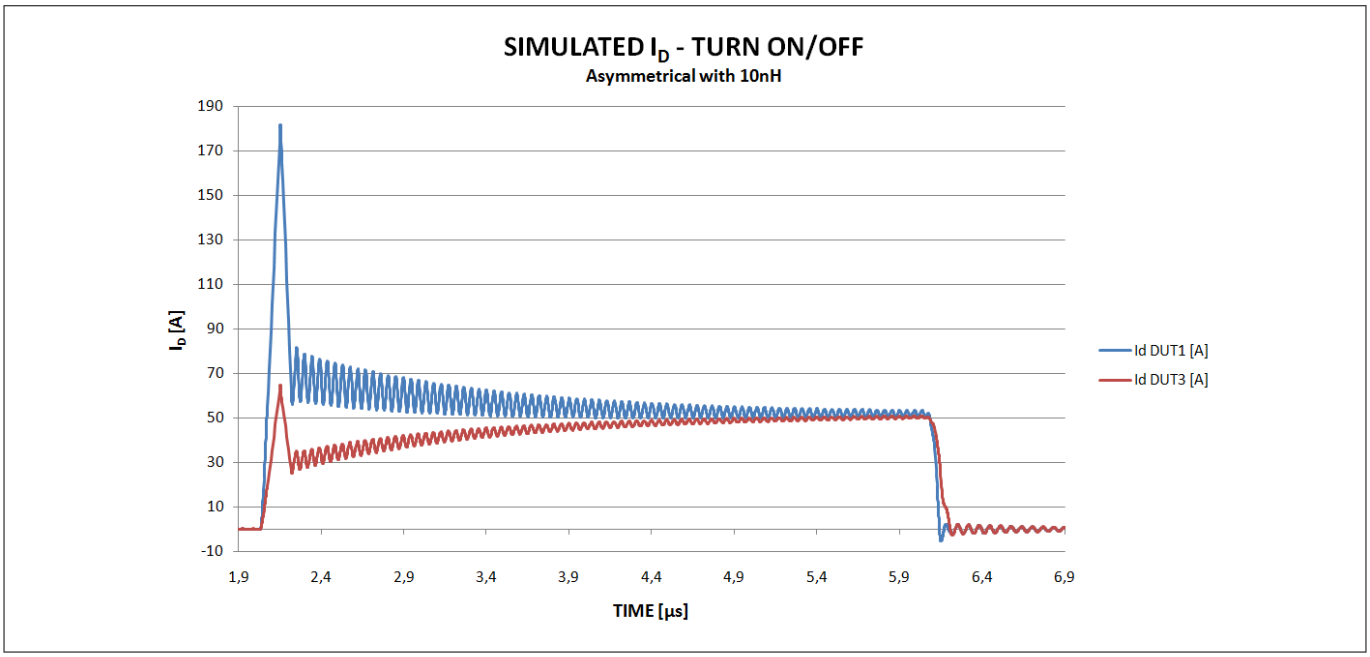

Figure 21 Asymmetrical current partitioning (10 nH inductance)

4 Analysis

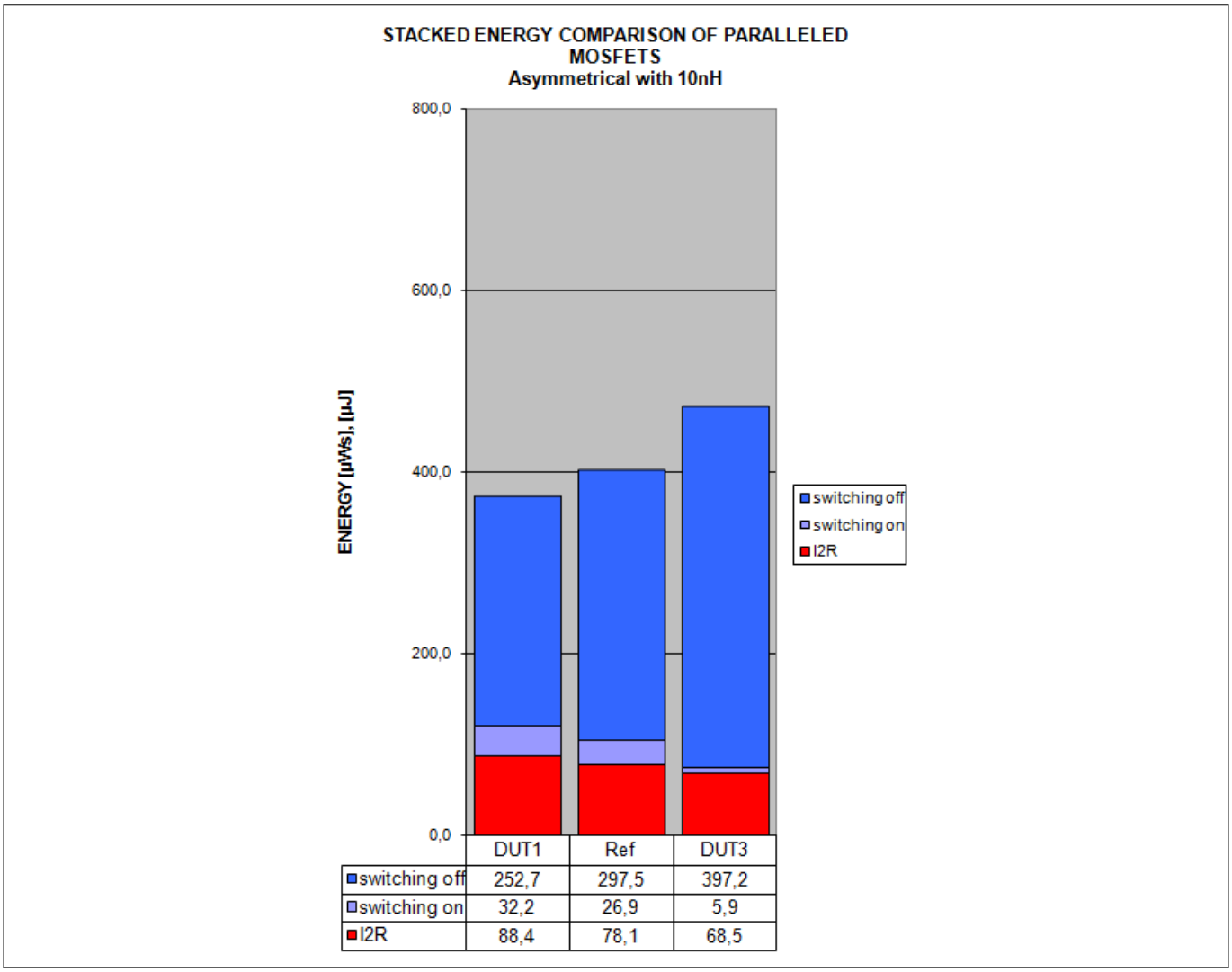

Figure 22 Losses in an asymmetrical layout

5 Summary

The simulations and measurements show the differences in the losses.

The biggest variation can be seen if the V_{GSth} shows the worst-case figures.

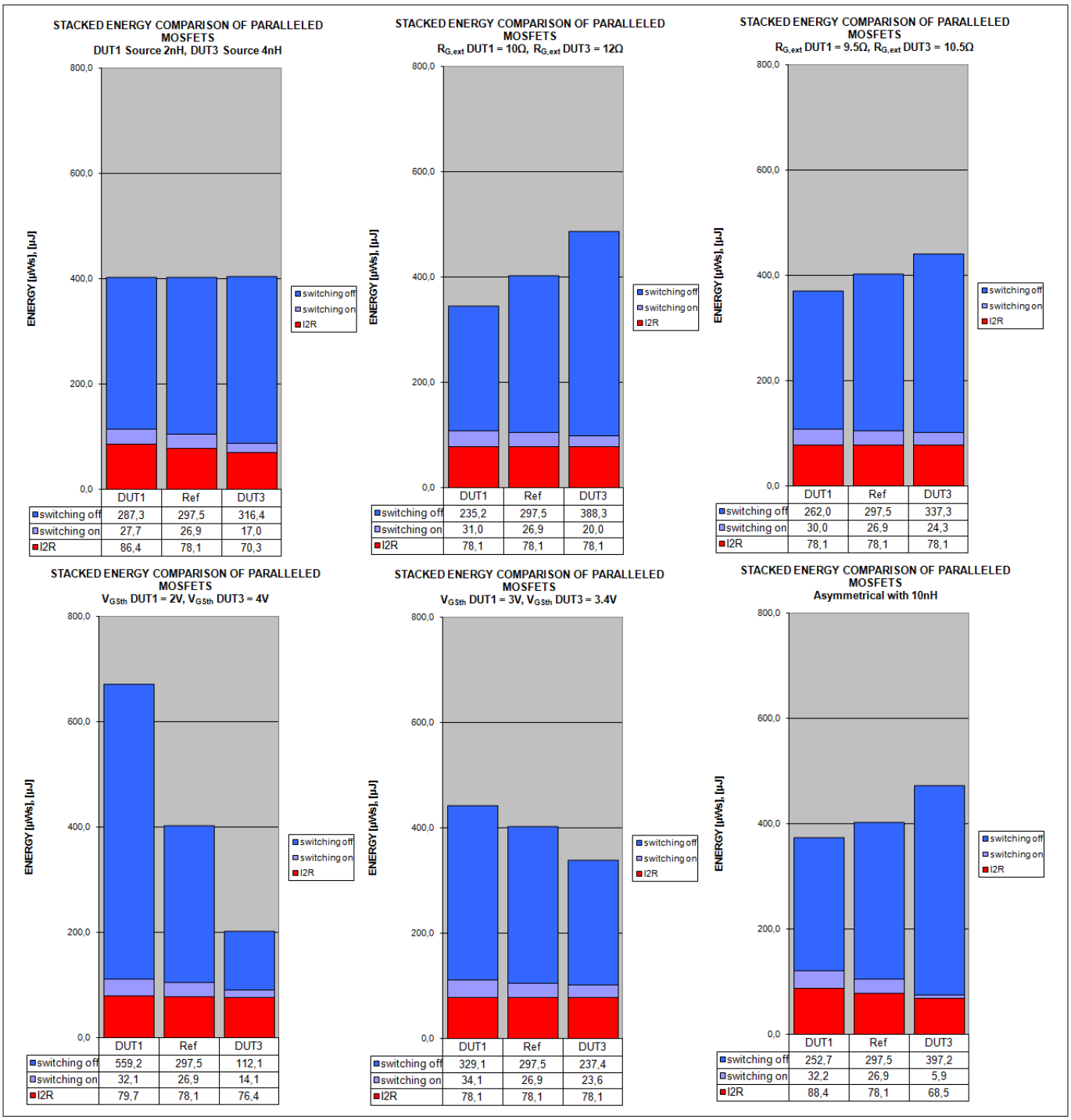

Figure 23 Losses overview

6 Revision history

Document version	Date of release	Description of changes

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